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Performance of the VAX-11/780 translation buffer: simulation and measurement

Authors: Douglas W. Clark and Joel S. Emer | Authors Info & Claims

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Abstract

A virtual-address translation buffer (TB) is a hardware cache of recently used virtual-to-physical address mappings. The authors present the results of a set of measurements and simulations of translation buffer performance in the VAX-11/780. Two different

misses. Additional hardware measurements were made with half the TB disabled. Trace-driven simulations of several programs were also run; the traces captured

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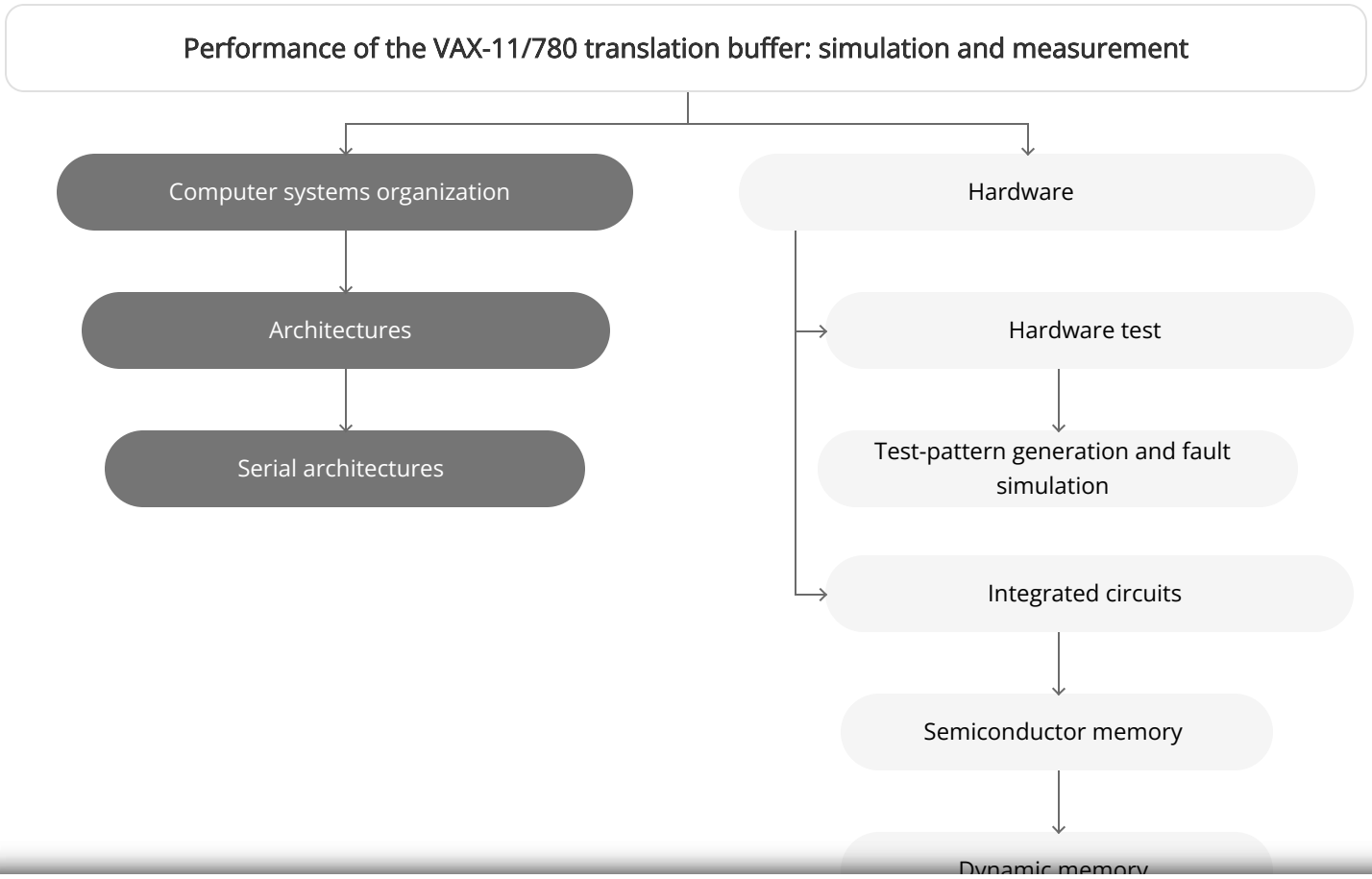
Index Terms



Nine solutions to the cache consistency problem for shared-memory multiprocessors with multiple translation-lookaside buffers (TLBs) are described. A TLB's function is defined, and it is shown how TLB inconsistency arises in uniprocessor an...

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focused on how to minimize buffer misses and the caused performance degradation. However, the side effects and...

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