

The case for the reduced instruction set computer

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INTRODUCTION

One of the primary goals of computer architects is to design computers that are more cost-effective than their predecessors. Cost-effectiveness includes the cost of hardware to manufacture the machine, the cost of programming, and costs incurred related to the architecture in debugging both the initial hardware and subsequent programs. If we review the history of computer families we find that the most common architectural change is the trend toward ever more complex machines. Presumably this additional complexity has a positive tradeoff with regard to the cost-effectiveness of newer models. In this paper we propose that this trend is not always cost-effective, and in fact, may even do more harm than good. We shall examine the case for a Reduced Instruction Set Computer (RISC) being as cost-effective as a Complex Instruction Set Computer (CISC). This paper will argue that the next generation of VLSI computers may be more effectively implemented as RISC's than CISC's.

As examples of this increase in complexity, consider the transitions from IBM System/3 to the System/38 [Utley78] and from the DEC PDP-11 to the VAX11. The complexity is indicated quantitatively by the size of the control store; for DEC the size has grown from 256 x 56 in the PDP 11/40 to 5120 x 96 in the VAX 11/780.

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ance in speeds; it is not clear that architects have asked themselves whether this imbalance still holds for their designs.

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