Tutorial on Cadence Innovus Implementation System

EE 201A – VLSI Design Automation – Spring 202

UCLA Electrical Engineering

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Based on slides from Mark Gottscho, Vishesh Dokania
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Innovus

- Industry standard physical design suite for complete netlist (post-synthesis) to GDSII flow.
- 2016 version of the traditional Cadence Encounter P&R tool.
- Sophisticated proprietary algorithms, iterative PPA optimization
- Lots of knobs on various commands for designer optimization
- GUI interface + TCL scripting

Tool Setup & Run

- Setup

```
$ source
/w/class.1/ee/ee201o/ee201ot2/csh_ee201a_setup
```

- Run with GUI

```
$ innovus
```

Without GUI

```
$ innovus -nowin
```

- Run Tcl script from Innovus window

```
innovus 1> source lab4_skeleton.tcl
```

- Alternatively, directly run Tcl script when starting Innovus (with or without GUI)

```
$ innovus -win -init lab4_skeleton.tcl
```

- Redraw current design
  - Ctrl + r

Doc Location

- Innovus - Docs located at:

```
/w/apps3/Cadence/INNOVUS161/doc/{innovusUG,
innovusTCR}
```

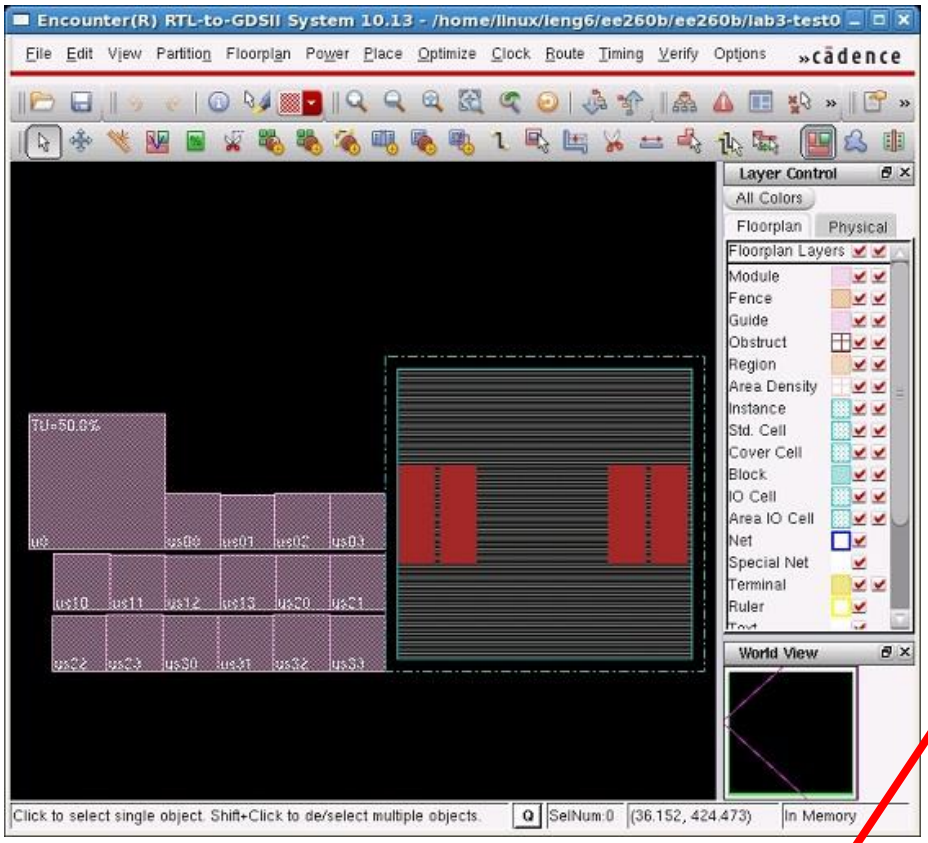
UG = User Guide

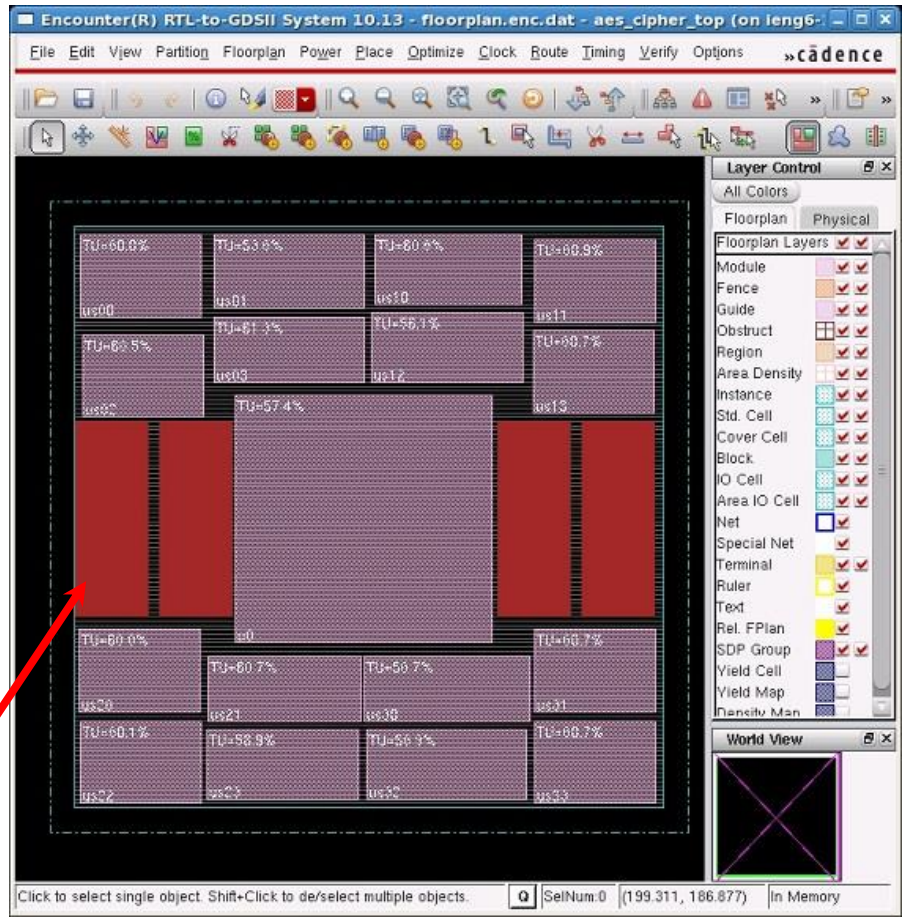
TCR = Text Command Reference

- Note:
  - Images on following slides do not exactly correspond to the specific command outputs
  - Only meant to help visualize the general idea.

Floorplanning

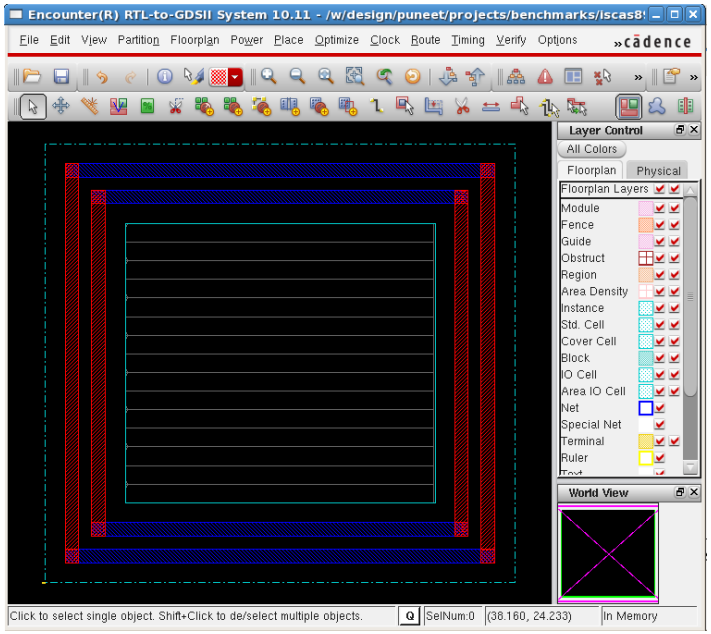
```
# Specify floorplan dimensions / cell utilization
floorplan -r aspectRatio rowDensity [coreToLeft coreToBottom coreToRight
    coreToTop]
```



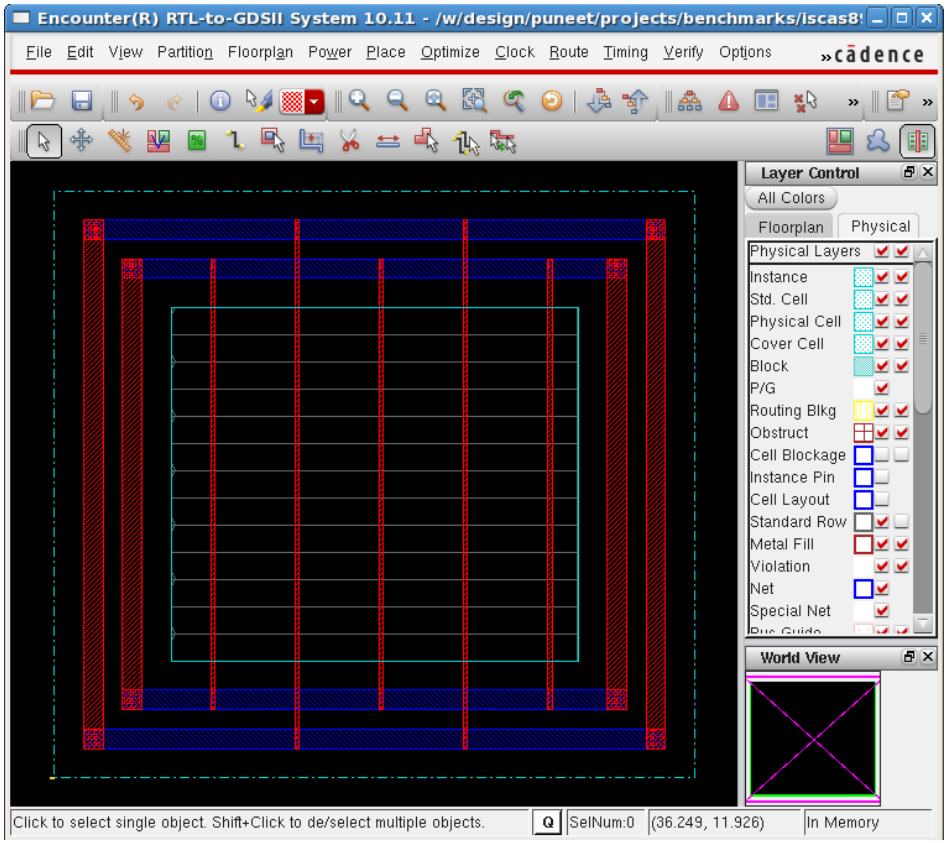


Hard macros

Power Structure



Stripes

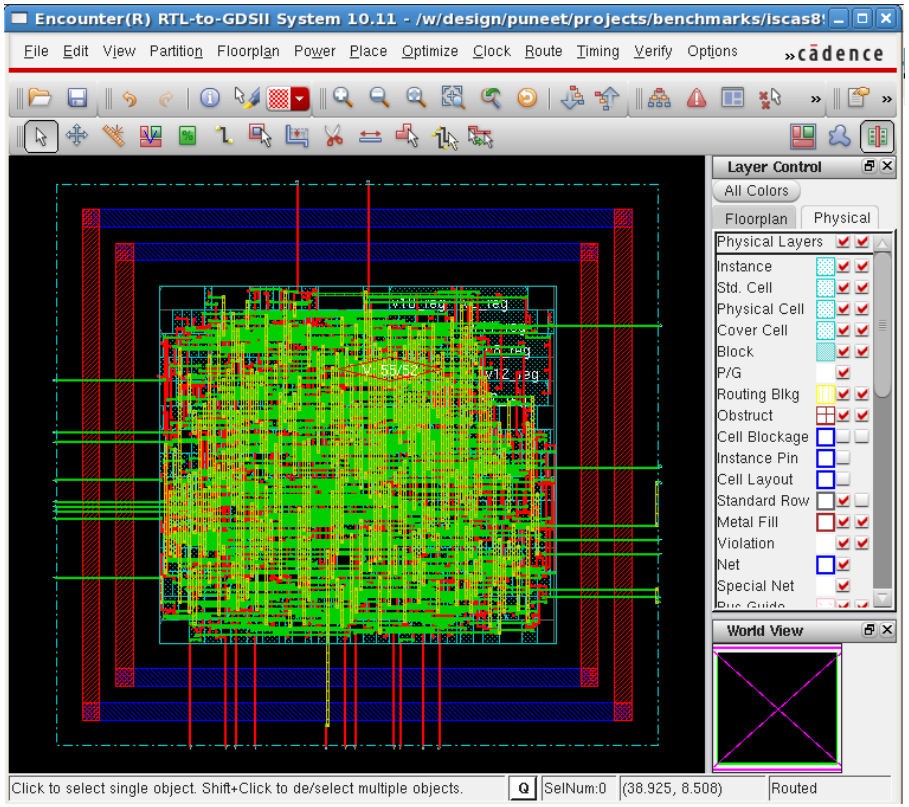


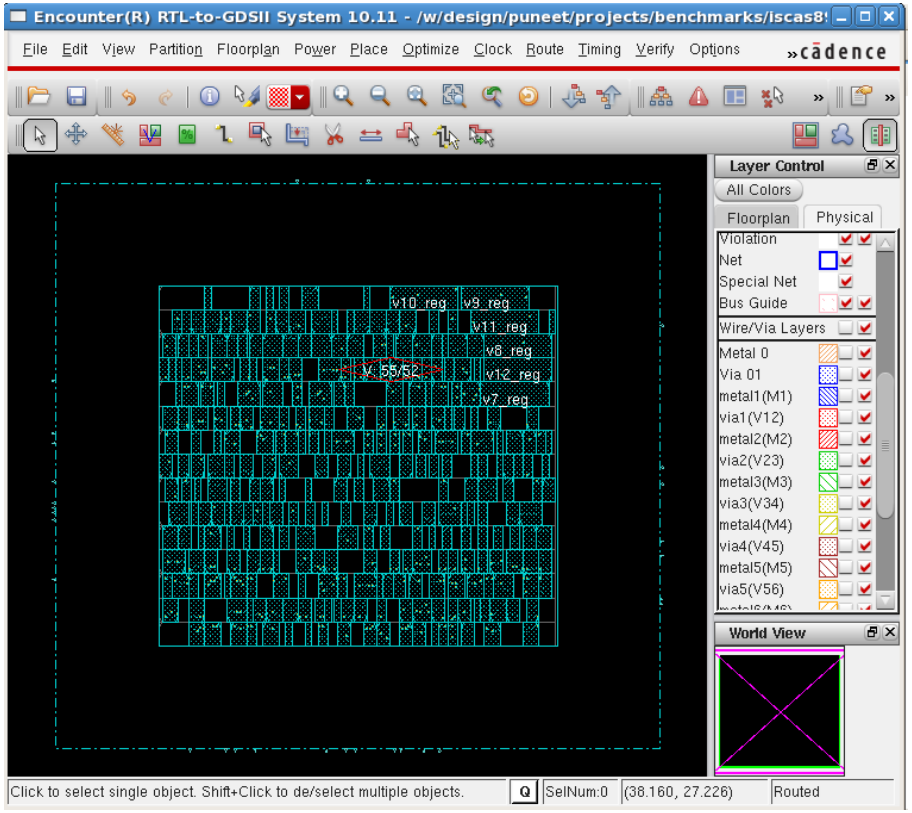
- E.g., Rings with 1 micron width and spacing with M1 in horizontal and M2 vertical:

```
addRing -layer {top metal1 bottom metal1 left metal2
right metal2} -spacing {top 1 bottom 1 left 1 right 1} -
width {top 1 bottom 1 left 1 right 1} -center 1 -nets {
VDD VSS }
```

Placement

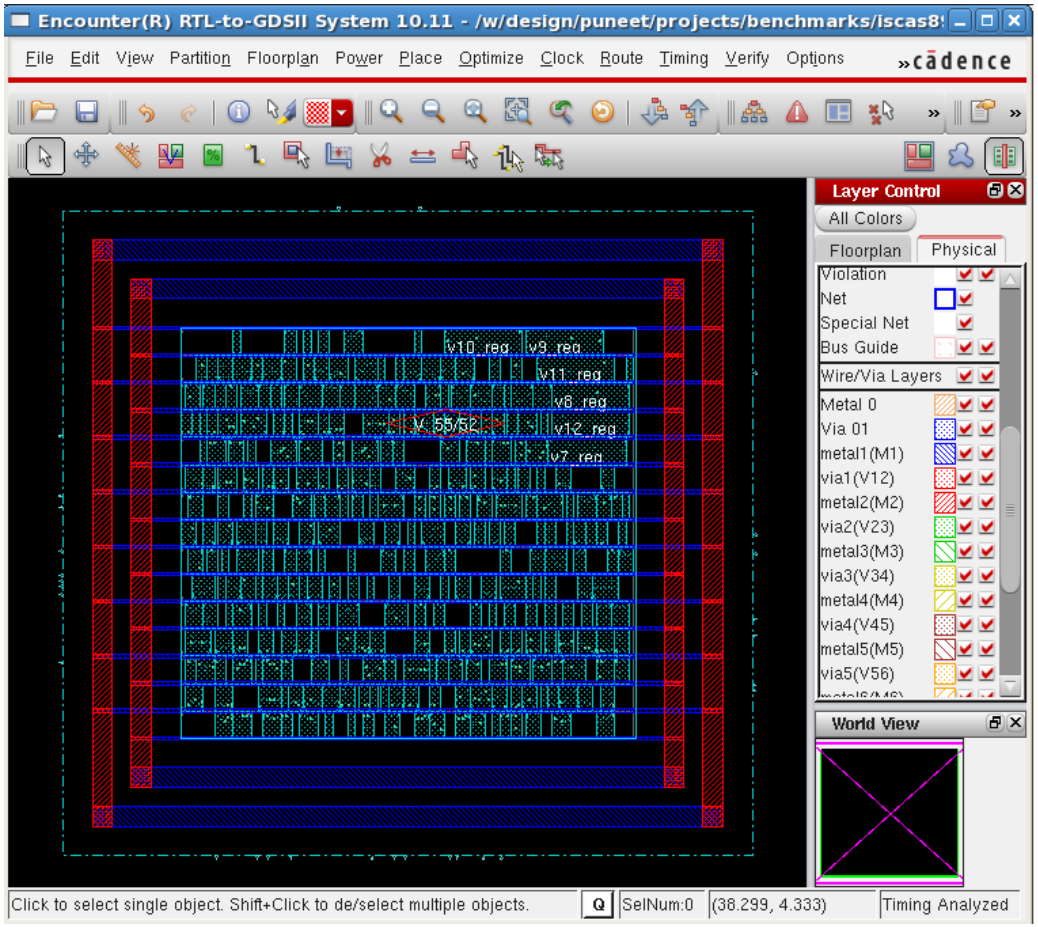
- `placeDesign` #timing-driven by default





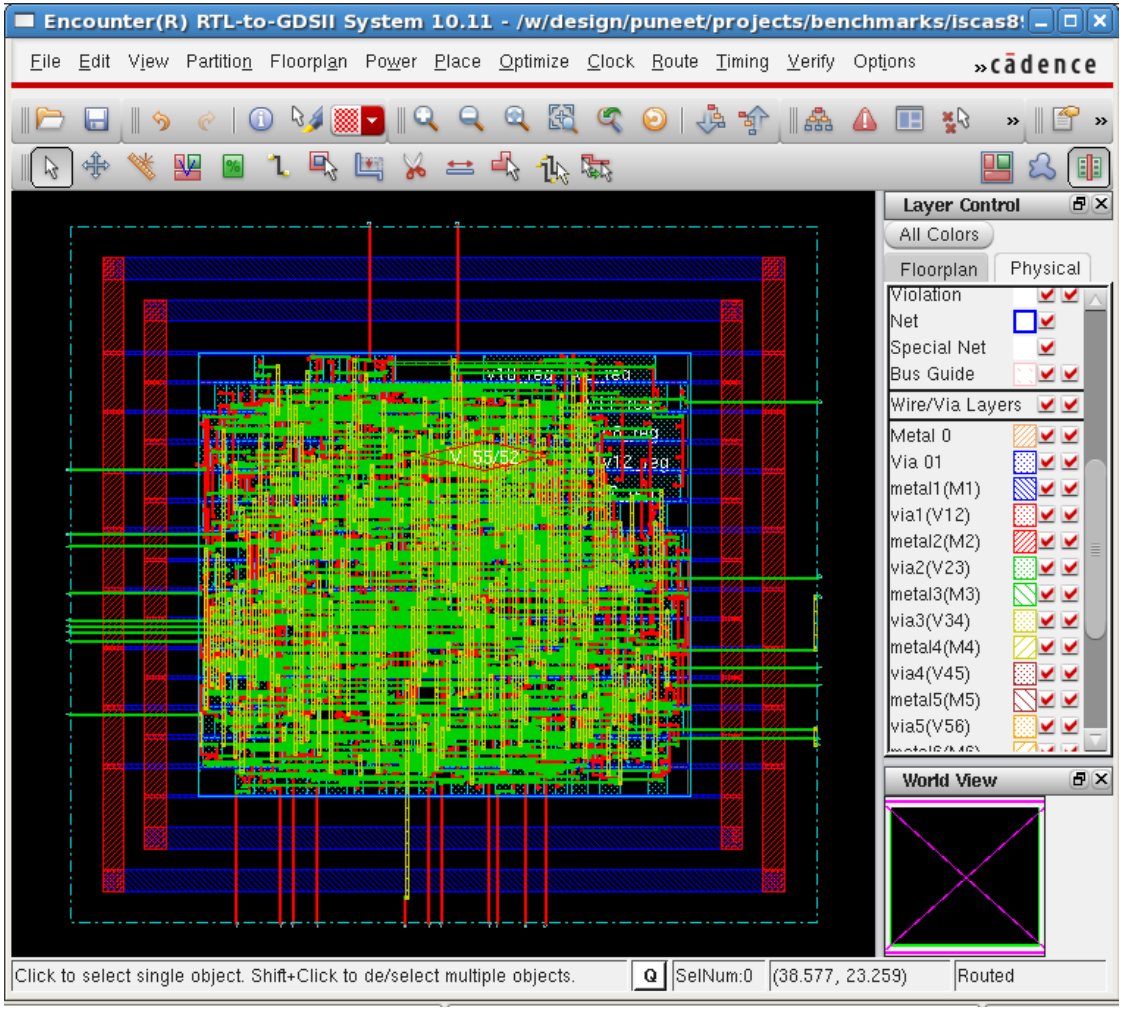
Special Route power nets

- `sroute -connect { corePin } -corePinTarget { firstAfterRowEnd } -nets { VDD VSS }`



Quick Cap/Congestion Estimation with Trial Route

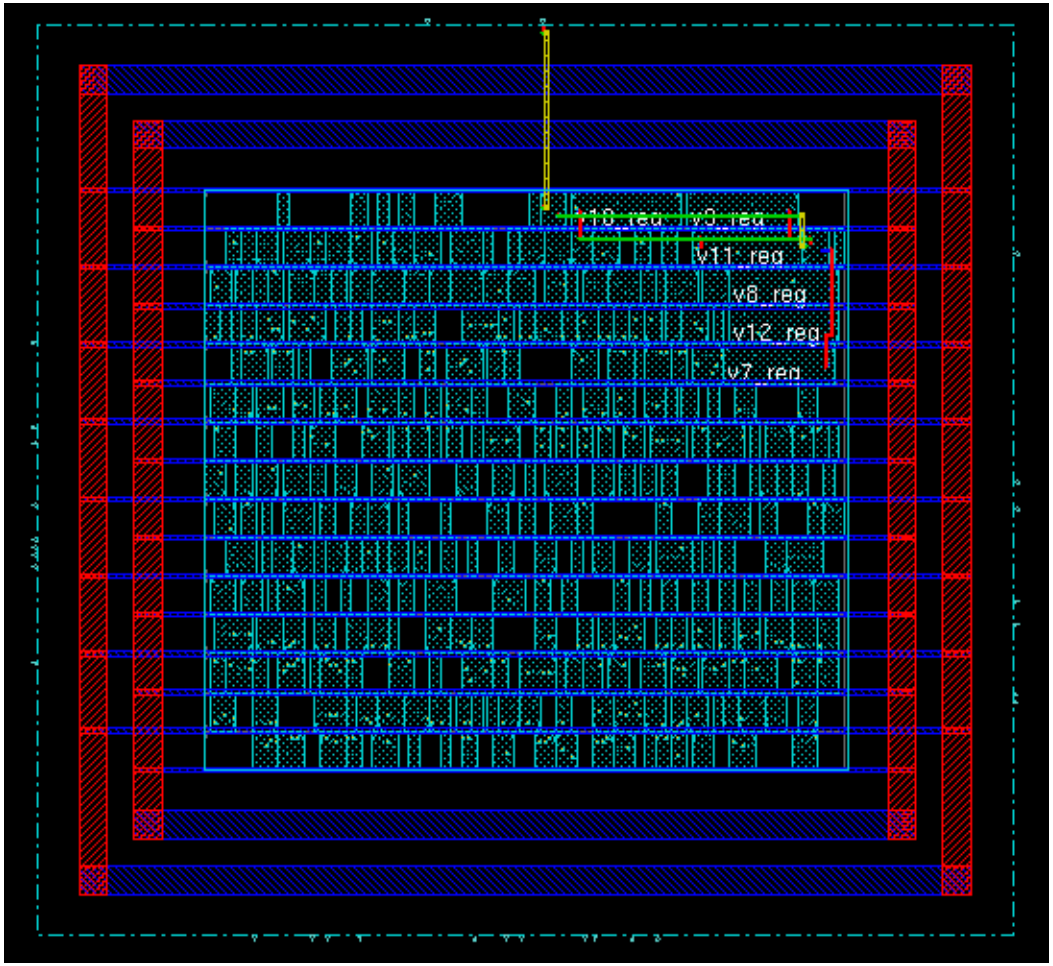
- `trialroute` # quick global + detailed routing



Clock Tree Synthesis

- `set_ccopt_property buffer_cells {BUF_X1 BUF_X2}`
  `set_ccopt_property inverter_cells {INV_X1 INV_X2 INV_X4 INV_X8 INV_X16}`
- `create_ccopt_clock_tree_spec`
- `ccopt_design -cts`

- Builds clk tree
  Resizes instances
  Detail-Routes clk tree



Global Routing (globalRoute)

Congestion Analysis: (blocked Gcells are excluded)

Layer	OverCon #Gcell (1-2)	OverCon #Gcell (3-5)	OverCon #Gcell (6-7)	OverCon #Gcell (8-10)	%Gcell OverCon
Metal 1	0(0.00%)	0(0.00%)	0(0.00%)	0(0.00%)	(0.00%)
Metal 2	15(12.2%)	7(5.69%)	16(13.0%)	16(13.0%)	(43.9%)
Metal 3	20(15.2%)	8(6.06%)	0(0.00%)	0(0.00%)	(21.2%)
Metal 4	8(6.06%)	0(0.00%)	0(0.00%)	0(0.00%)	(6.06%)
Total	43(8.98%)	15(3.13%)	16(3.34%)	16(3.34%)	(18.8%)

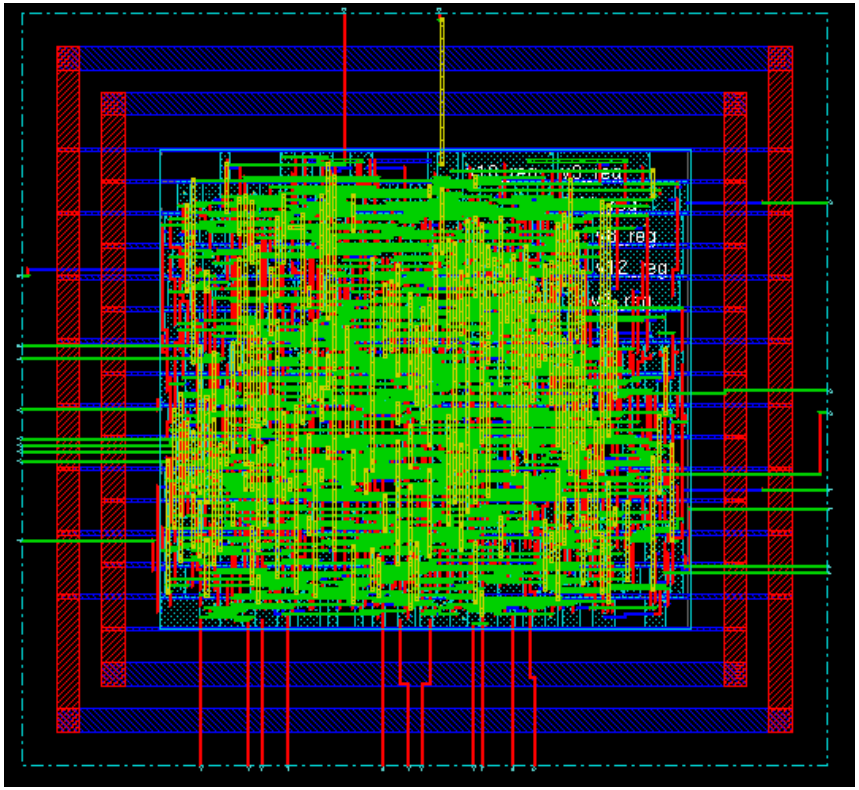
The worst congested Gcell overcon (routing demand over resource in number of tracks) = 10

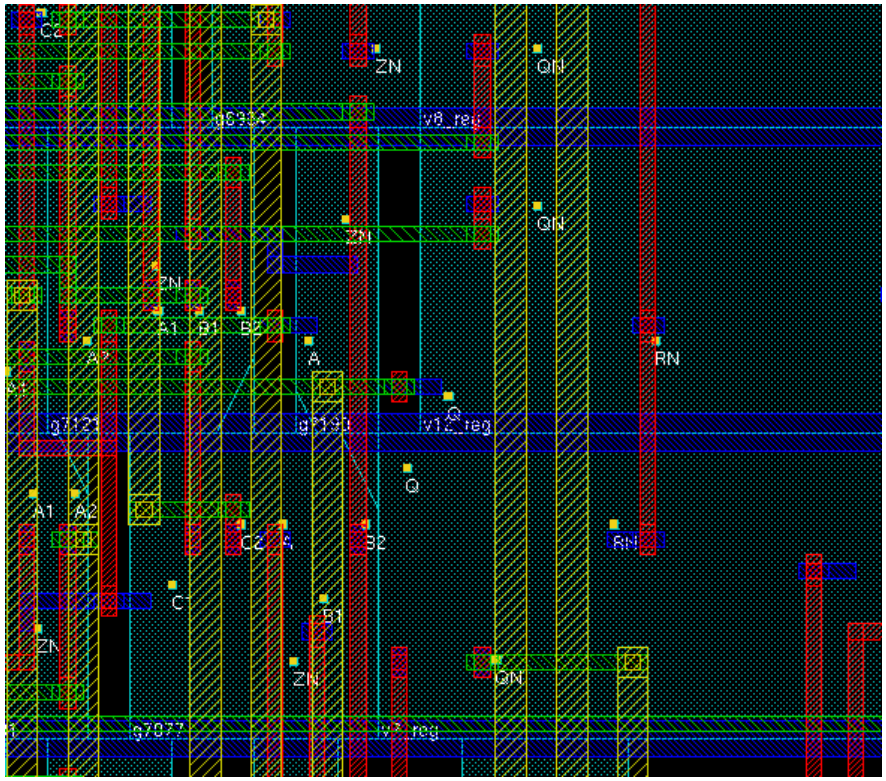
```
Total wire length = 5676 um.
Total half perimeter of net bounding box = 2699 um.
Total wire length on LAYER metal1 = 70 um.
Total wire length on LAYER metal2 = 1458 um.
Total wire length on LAYER metal3 = 2645 um.
Total wire length on LAYER metal4 = 1502 um.
Total wire length on LAYER metal5 = 0 um.
Total wire length on LAYER metal6 = 0 um.
Total wire length on LAYER metal7 = 0 um.
Total wire length on LAYER metal8 = 0 um.
Total wire length on LAYER metal9 = 0 um.
Total wire length on LAYER metal10 = 0 um.
```

```
Total number of vias = 1879
Up-Via Summary (total 1879):

-----------------------
  Metal 1          841
  Metal 2          676
  Metal 3          362
-----------------------
                  1879

Max overcon = 10 tracks.
Total overcon = 18.79%.
Worst layer Gcell overcon rate = 21.21%.
```

Routing

- `globalRoute` #global only
  `detailRoute` #detailed only
  `globalDetailRoute` #global and detailed routing





Outputs

- Timing, Power, Area reports at various flow stages
- Internal Innovus rule checks
  - `verifyGeometry` (DRC estimate)
  - `verifyConnectivity` (LVS equivalent)
  - True LVS and DRC checks in tools like Calibre
- DEF – `defOut`
- SPEF – `rcOut -spef`
- Optimized Verilog netlist - `saveNetlist`
- Import-able Innovus format - `saveDesign`
- Final GDSII – `streamOut`
  - Requires GDS of individual std cells, layer map