Lecture

18

ECE M216A

Test

Prof. Dejan Marković

ee216a@gmail.com

Definitions

Controllability:

the ability to *set* the state of internal nodes from the chip's input pads

Observability:

the ability to *propagate* the state of internal nodes to the chip's output pads

Design for Test and Debug

The art of adding functionality to the chip

to enhance its controllability and observability

so that it can be effectively debugged

and tested for correct operation

Silicon debugging is a growing problem that accompanies the increasing complexity of current designs

Discussion Topics

- **How chips fail**
- **Chip test and debug**

Reading

- W&H: Chapter 9

Most slides in this lecture are from:
Shannon Morton, (SGI), ISSCC 2003

People Got Fired Over This

Antenna at the bottom (covered when you talk)

Technology Scaling: The Dark Side

- **1µm to 0.1µm**
  ⇒ 100x increase in complexity of internal state

- **Die size also increasing**
  ⇒ even more states

- **Only a small *relative* increase in the number of pins available for test**

- **Longer lengths of interconnect (over a mile!)**
  - More layers & tighter pitches ⇒ more IC faults

Complexity

- A combinational logic with N inputs
  implies 2^N test vectors

- A sequential logic with N inputs and M states
  implies 2^{N+M} test vectors

Cost of Testing

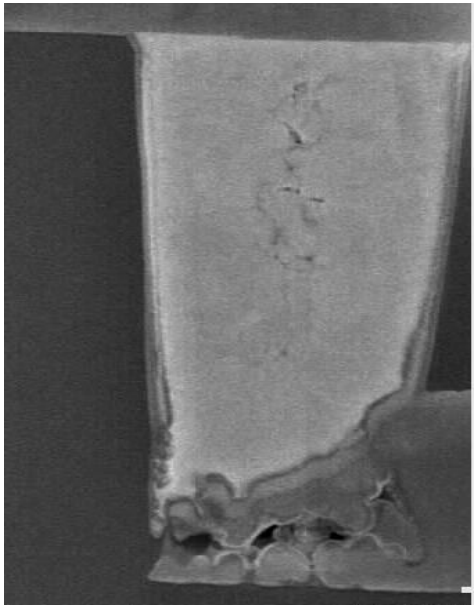
- **Man-hours required to generate sufficient test coverage (if at all possible) is *vastly* increased**
- **Testing occurs at different stages and costs differently**
  - Wafer, packaged chip, board, system, field
  - 10x more expensive at each level
    (wafer probing is $0.1/unit)
- **Each part requires more time/tester, or more testers**
  - 50M units at 1sec/unit $\Rightarrow$ $5 million/year
  - At least *$2-3 million* for a 1000-pin tester
  - Reduced volume $\Rightarrow$ unable to meet demand
    $\Rightarrow$ loss of potential revenue

Why Chips Fail?

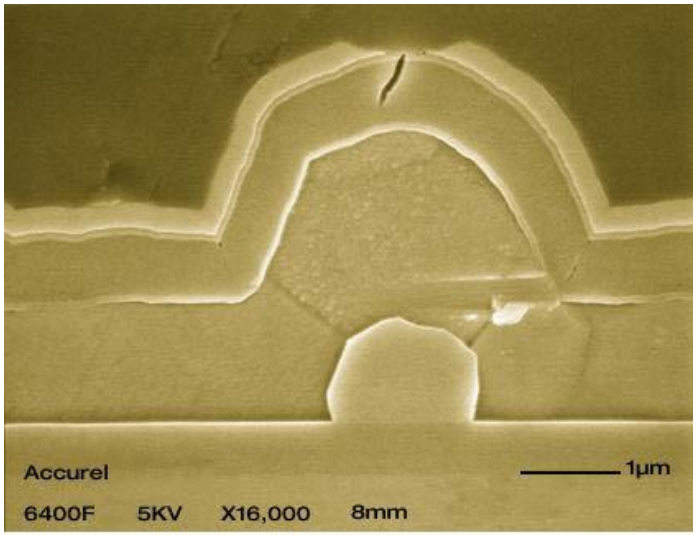
- Process defects
- Reliability failures
- Iddq failures
- Timing and noise failures
- Soft errors
- Logic design failures

Process Defect Examples

- **Missing or poorly formed via (*infant mortality*)**



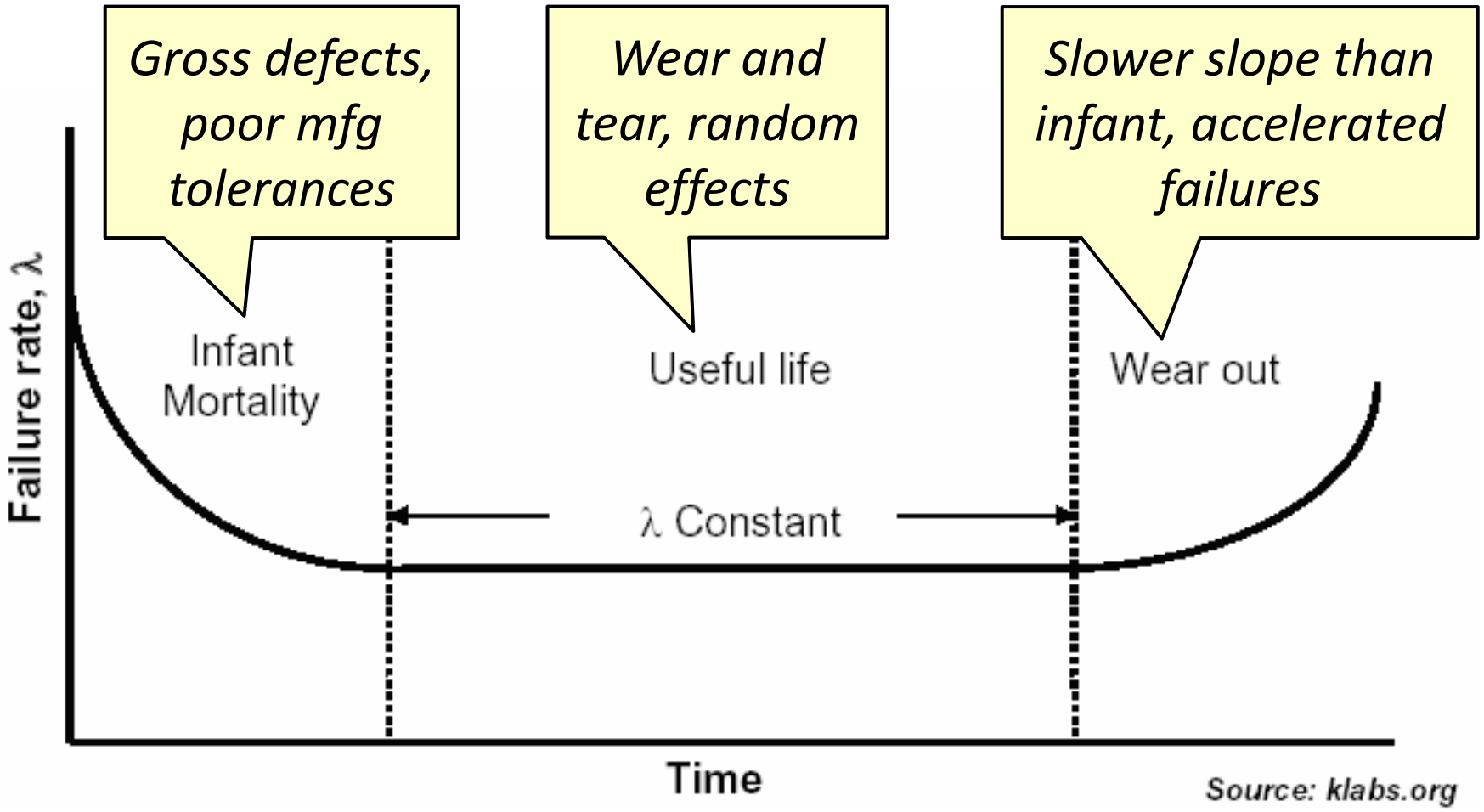
- **Hillock causing an open in upper layer metal**



Failure Analysis Fig 1: IC cross-section: HIllock in metal caused high stress in passivation and lead to cracks and partial popping of top layer.

- **Some causes of process defects**
  - Dust particles, Oxide/Si defects/impurities/roughness
  - Lithographic errors, Temp & chemical composition of processes

Reliability

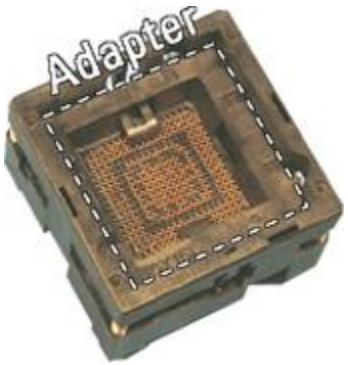


Burn-in Oven Boards

- **Populate a burn-in board with your parts**
  - Board exercises the parts during burn-in

V_{DD} : 1.5-2x
T : 150-200°C

- **High-power chips strain the capacity of burn-in ovens**
  - Can't put too many 100W and 100A chips on a burn-in board!



www.sensata.com

www.aiaaoc.com

www.xbitlabs.com

Iddq Failures

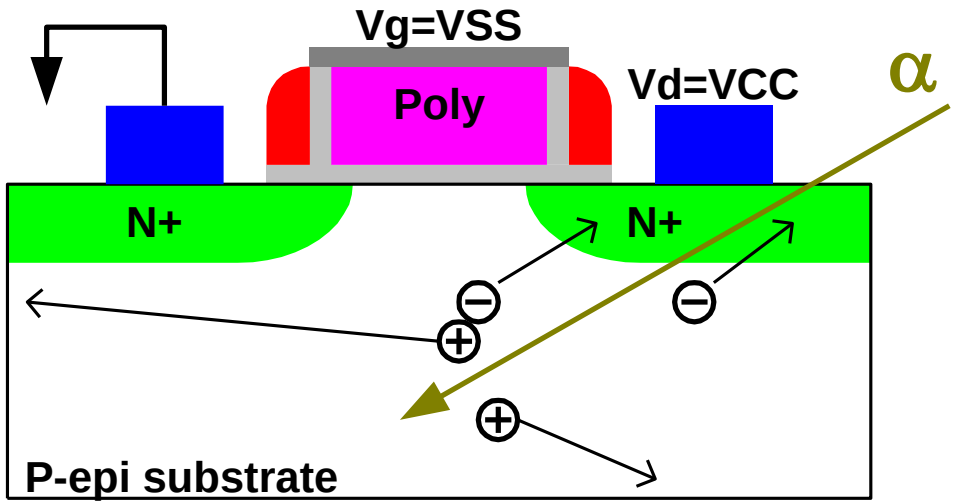
- **Excessive standby current (through S/D & gate too)**
  - Beyond that expected from sub-threshold leakage
    - Pseudo-nmos structures (typically disallowed)
    - Current references (analog circuitry)
  - May indicates process defect having caused a short
- **Tested during bring-up & burn-in**
  - May become less relevant as leakage (sub-V_T & gate) is increasing rapidly with each technology
    - May also be swamped by large L2/L3 SRAM leakage

Timing & Noise Failures

- **Unforeseen critical path on chip**
  - Perhaps only under certain bizarre conditions
  - **Example:** Insufficient differential into low-swing SA's
  - Particularly relevant to shrinks (interconnect scaling)

- **Glitch resulting from excessive RLC noise**
  - Timing push-out to await settling of glitch
    - Perhaps only under certain bizarre conditions
  - Functional failure if driven into state-holding circuitry
  - Reliability failure due to excessive coupling

Soft Errors: What are they?

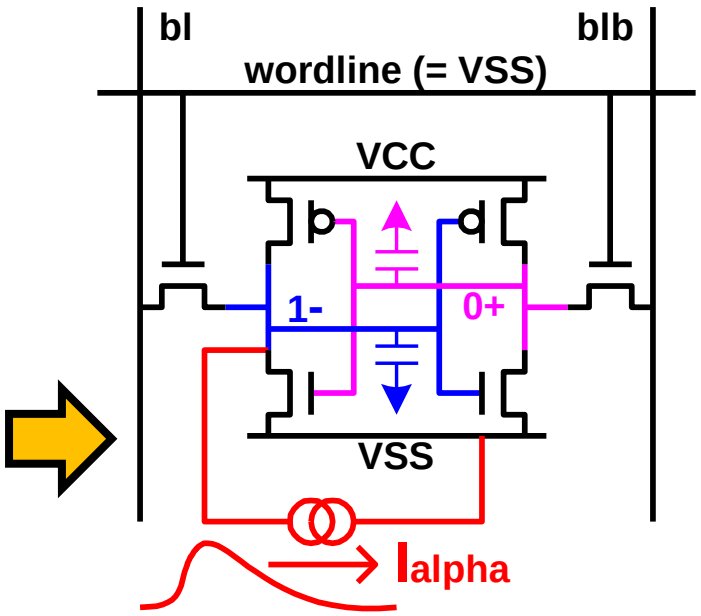


- **Alpha particle's (He nucleus) released primarily from radio-active isotopes in lead (C4 bumps)**
  - Cosmic rays of ≈GeV energy levels
- **Collisions with Si atoms generate e^-/hole pairs**
- **e^- are swept across PN junction reducing V_d**

Soft Errors - Memory

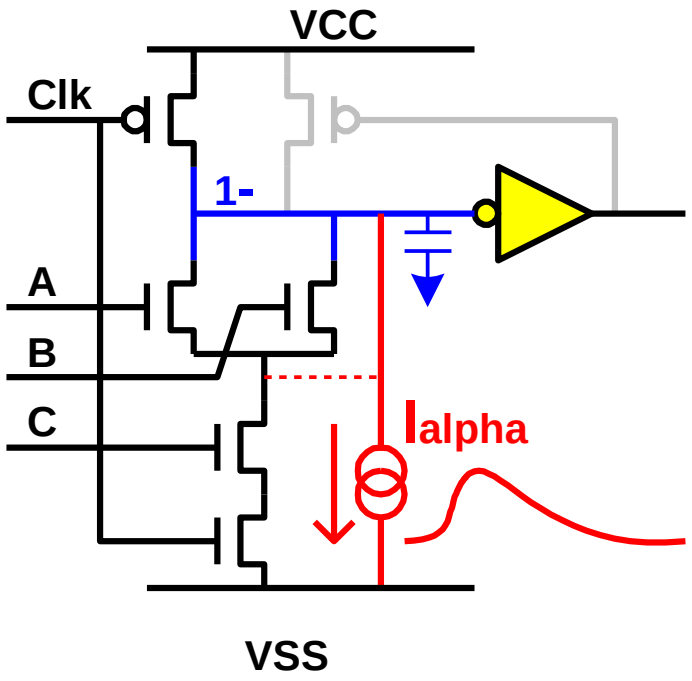
- **Memory is usually the focus**
  - Dense, low capacitance

Inject current into S/D region and measure how much charge (Q_{crit}) is needed to flip the cell



- **ECC codes employed on large arrays to enable sufficient detection and correction**
- **Parity checks used to enable sufficient detection**
- **C4 bumps may be prohibited over arrays, but...**

Soft Errors - Logic



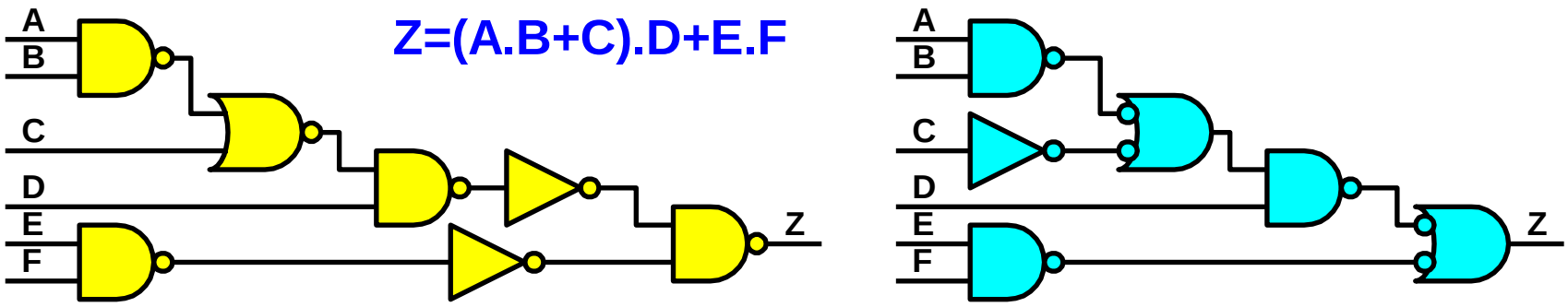
- **Logic is also prone to soft errors:**
  - Dynamic nodes and latches may flip state
  - Static nodes may create a glitch that gets latched

- **If ECC is employed on the arrays, even with C4 bumps over them, then logic soft-errors may govern overall FIT rate (failures in 10^9 hours)**

Logic Design Failures (Debug)

- **Incorrect wiring into a gate**
- **Incorrect gate in a logic function**
- **Incorrect algorithm in the micro-architecture**

- **BUBBLE ERRORS!**
  - Particularly between top or 2nd-level blocks



VLSI Testing

- **Testing is expensive: VLSI testers cost $1-5M**
  - Volume manufacturing requires large number of testers
  - Test contributes 20-30% of the total chip cost

Step	Error Source	Test Type
Design	Design flaws	Design verification
Prototype	Design flaws Prototype flaws	Functional test (“silicon debug”)
Manufacture	Physical defects	Manufacturing test
Shipping	Mfg. test, transport	
System integration	Same	Functional test
Service	Stress, age	diagnosis

Courtesy: B. Nikolic

Testing Tools

- **Common "external" tools**
  - Probing
    - Land a probe onto a top metal square (10x10µm)
  - Imaging
    - Infrared – detect clock transitions
    - E-beam – reflected electrons from different-voltage wires are different
  - Iddq – monitor supply current
  - FIB – focused ion beam
    - Can cut or deposit metal to correct wiring (shorts, opens)
- **"Internal" tools**
  - Design features to aid test and debug

Functional Test

Employed as part of the bring-up flow to debug the chip's electrical, logical, and timing functionality

- **Evolving tests from basic ROM ⇒ Icache load & executing programs that fit wholly within caches**
- **To full multi-processor high-end applications in a variety of "real" user systems**
- **How do you identify the cause of a program failure?**
- **Explicit Design For Debug structures are helpful**

Chip design is becoming functionally sound

Debugging Concepts

- **Additional knobs available to debugging**
  - Raising and lowering the temperature
    - Simple lab – freeze spray and heat gun
  - Raising and lowering the supply voltage
  - Increase and decrease the cycle-time
    - Adjusting the duty cycle (clock compression)

- **Common fixes**
  - Slow logic – raise supply or increase cycle time
  - Race condition – increase temperature
  - Leakage – lower supply

Debugging a Chip

- **Run parts on tester, exercise the Clk shrink mechanisms**
  - Move clock edges to test speedpath theories

www.deniskitchen.com

- **Also vary the voltage and freq.**
  - Obtain "schmoo" plots
  - Named after the Li'l Abner comic strip (1940's)
    - One of the first schmoo plots looked round and bulbous

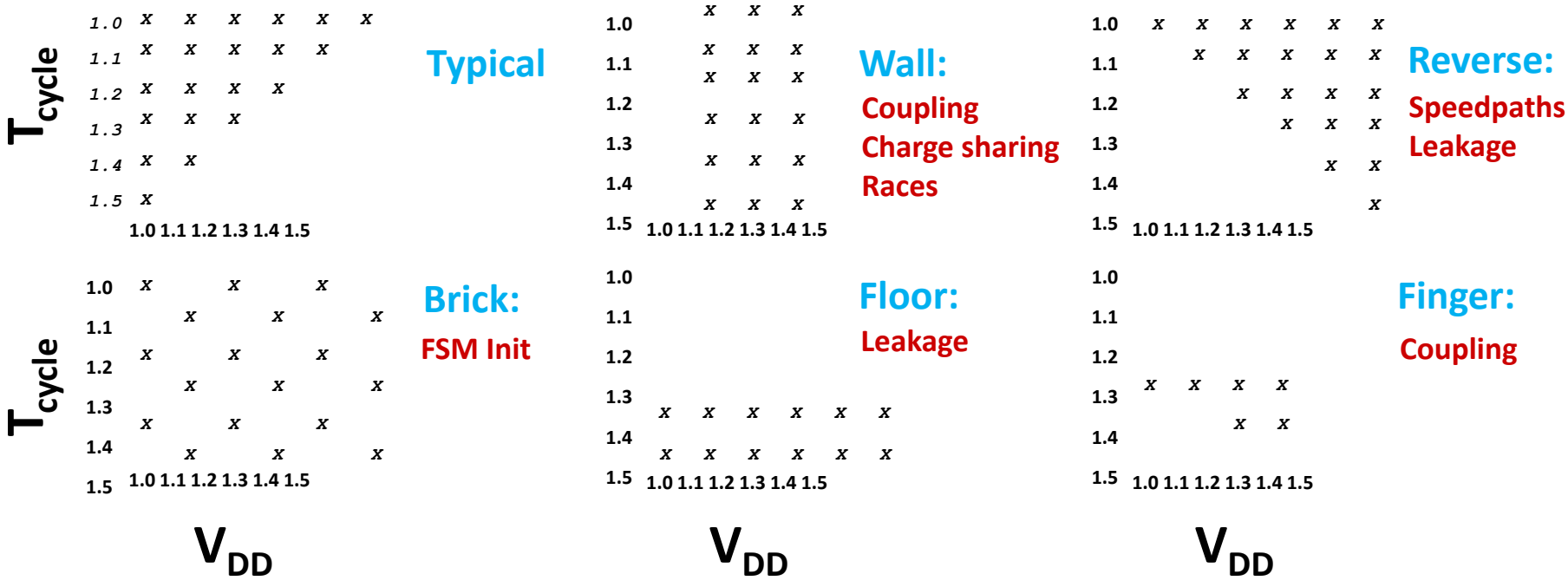
A "shmoo" (plural: shmoon)

Resembles a type of plot used by EEs
(who can't spell and call it a "schmoo")

Courtesy: M. Horowitz

Common Schmoos

- **Sweeping the supply and operating frequency (often at various temperatures)**
  - Selectively done as a manufacturing test
- **Can be an excellent way to determine problems**



Manufacturing Test

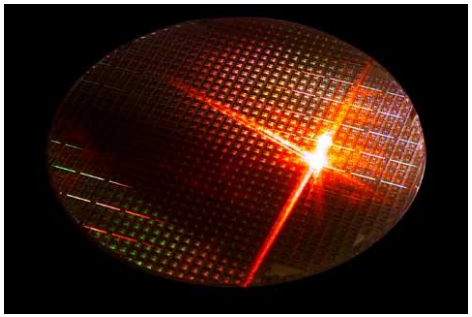
Employed as part of the production flow to screen out defective parts

- **Test patterns applied to the die/package to test for correctness against an ideal (fault-free) model**
  - May also test for basic delay faults/characterization
- **Burn-in tests to weed out parts that are prone to early failure (infant mortality) in the field**
- **Explicit Design For Test structures usually required**

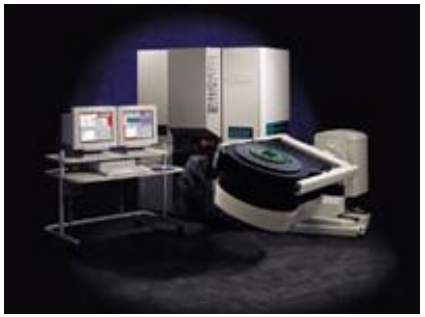
Chip design is already functionally sound

Manufacturing Test Flow

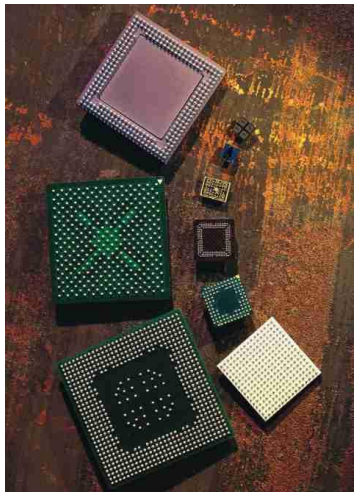
Raw Materials: *Sliced, polished, processed, according to a great design*



Wafer Probe: Probe card attached to ATE steps across each die: Basic functionality. Speed Paths.



Laser Repair: Zap fuses to enable redundant blocks & improve yield. Repeat wafer tests . Mark bad die.



Packaged Parts: Tests for more detailed functionality, speed binning.

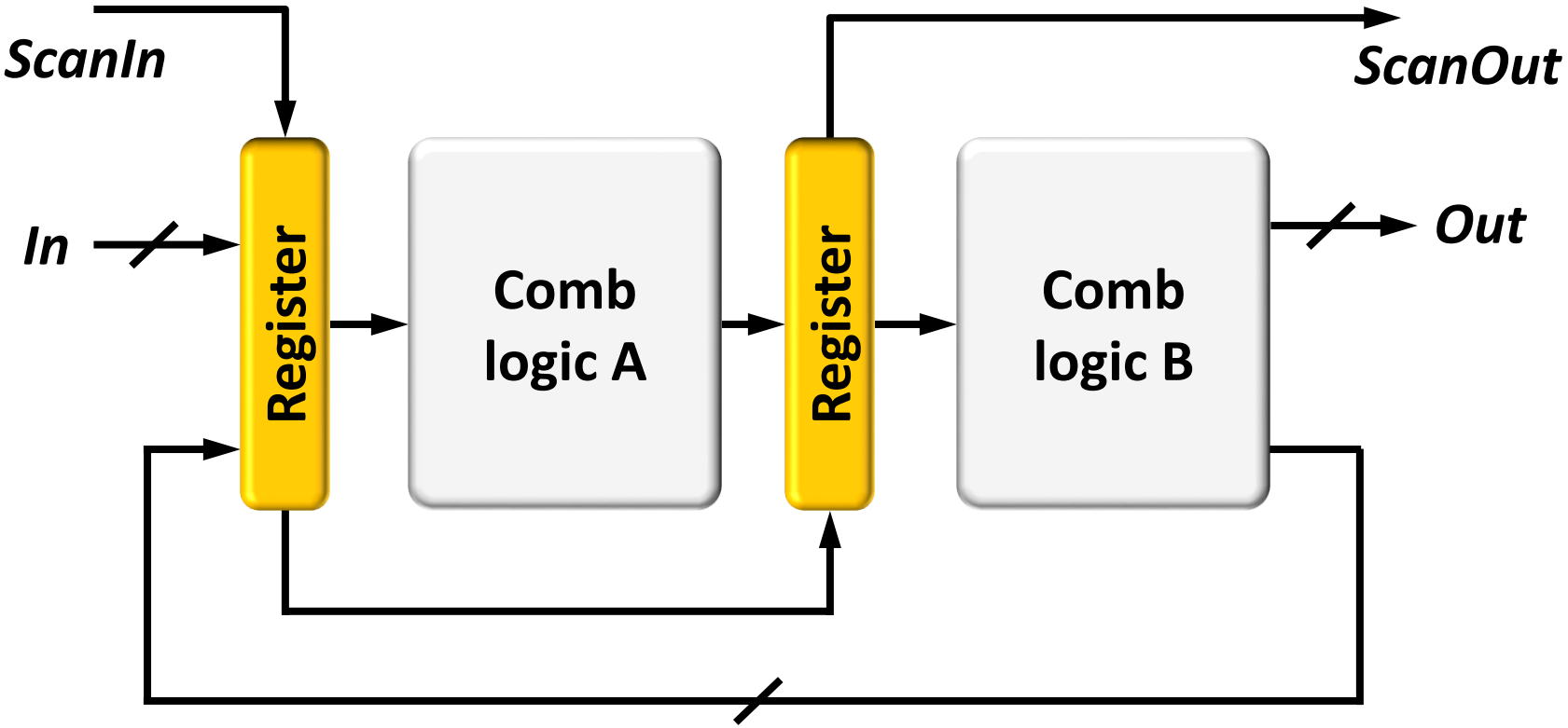
Burn-in: V/T stress over time, then re-test. Weeds out infant mortality failures.

System Test: Real apps, I/O, Power, Performance, etc.

Cost of Doing DFT

- **Increased area ⇒ less die/wafer & lower yield**
  - Increased cost per good die
  - Increased cap ⇒ hurts power & performance
- **Extra logic may be a part of the chip's critical path**
  - Reduced operating frequency ⇒ reduces revenue
- **Test logic itself has a risk of introducing a bug**
  - What tests the test logic?
- **The cost of doing DFT is far easier to quantify than the cost of not doing DFT**

Scan-based Test



- **Scan chains offer observability and controllability**
  - Can stop the chip and read out all the states
  - Can stop the chip and set all the states
  - Can trace back to find source of errors

Fault Models

Defects manifest in a variety of ways and may require the different circuit models to test for their presence

Fault Model	Effect on Circuit	Notes
Single stuck-at line	Single logic node stuck at 0|1	Most common
Multiple stuck-at lines	Multiple logic notes stuck at 0|1	Vast majority covered by SSL
Bridging	Logic node becomes AND(x,y) or OR (x,y) or X depending on driver strengths	May not be well covered by SSL
Delay	Gate of path delay is increased	
Coupling	Complex space-time dependence	Bitlines, buses, register files
Pattern sensitive	Complex space-time dependence	RAM arrays

ATG Time

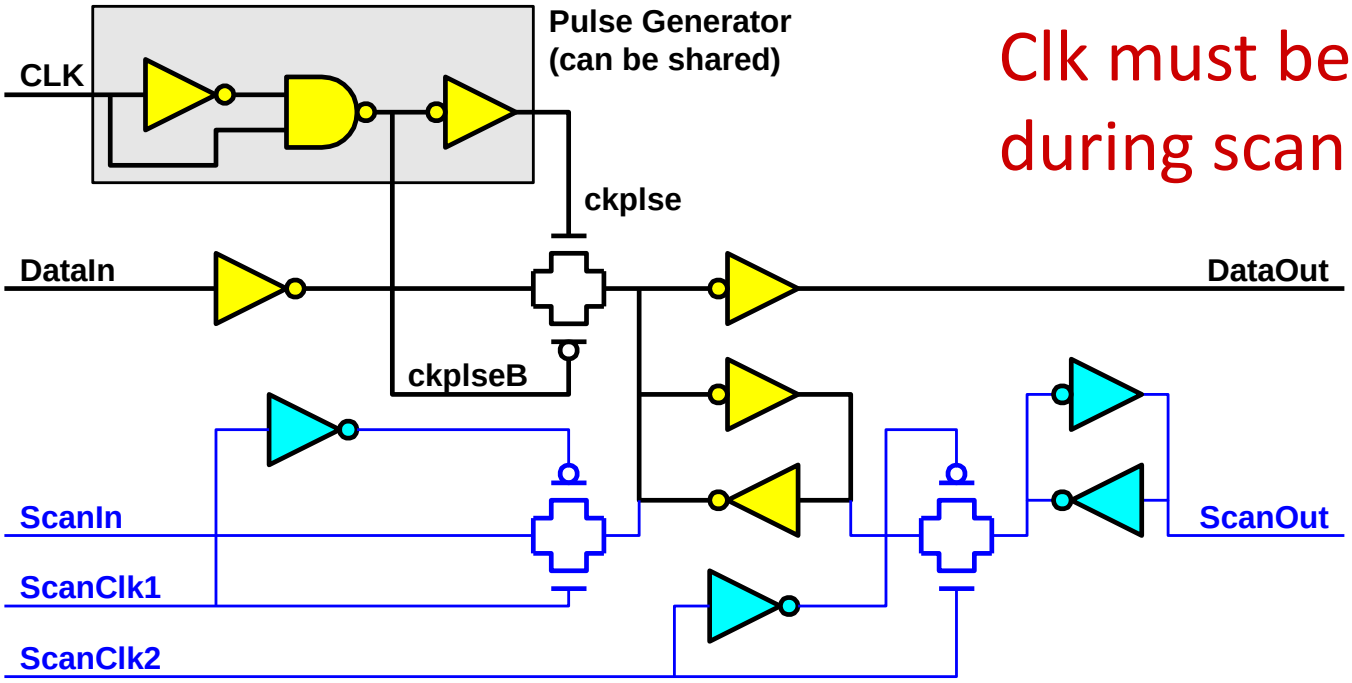
- **Time required to generate a test vector set for all SA faults is a function of:**
  - ATG technique & heuristics for decision-making
  - Number of Primary Inputs & Outputs
  - Number and size of sequential structures
  - Number of equivalent SA faults
  - Depth of logic from PI to PO (esp. for sequential!)

- **Circuits with ≈10^6 gates or ≈10^3 latches may be too large to test with suitable SA coverage and in a reasonable amount of time**

Scan Methodologies

- **Full Scan:** **Every latch in the design is a scan latch**
  - Do NOT scan simple pipeline stages
- **Partial Scan:** **A selection of latches are scannable**
  - Where low SA coverage is identified
  - Sequential logic: counters, data forwarding paths
  - Important data buses: PC, load/store bus
- **Scan Islands:** **No scan within blocks, but a ring of scan latches on the I/O surrounds the block**
  - More applicable to debug

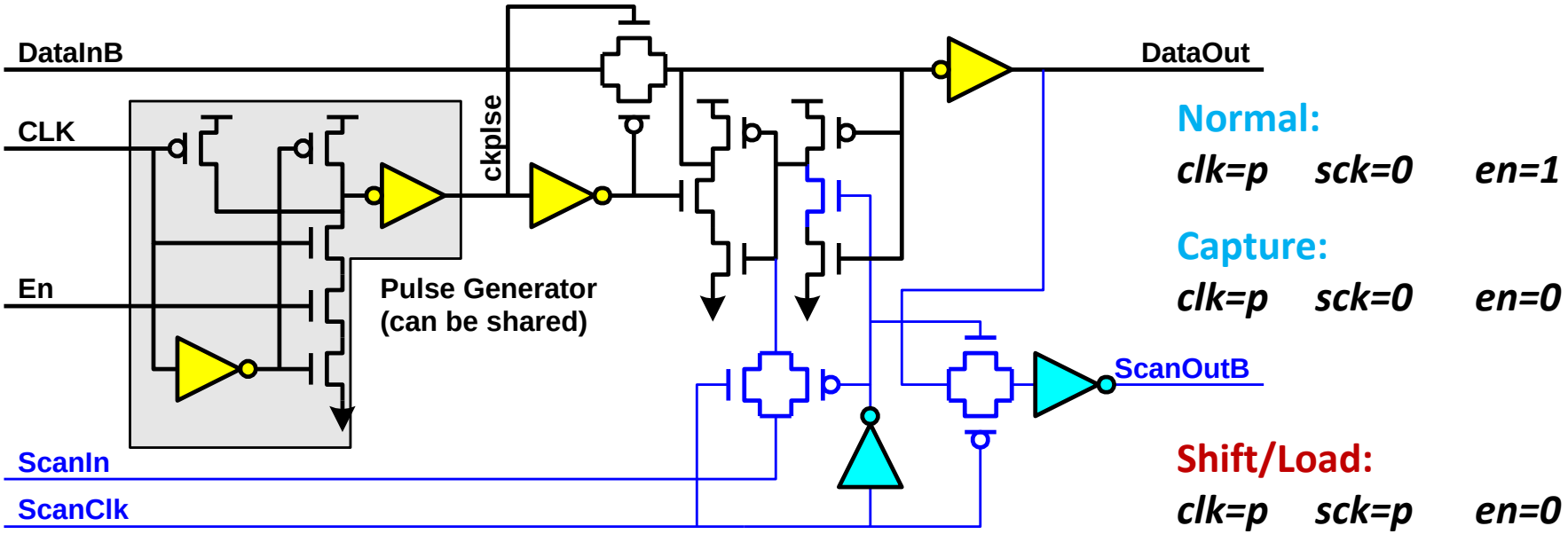
AMD's K6 Flip-Flop



Clk must be **inactive** during scan

- **Non-overlapping scan clocks ⇒ no race, easy to route**
- **No additional logic in the D→Q path ⇒ fast**
- **Shift is destructive (=Load)**

Intel's McKinley Flip-Flop



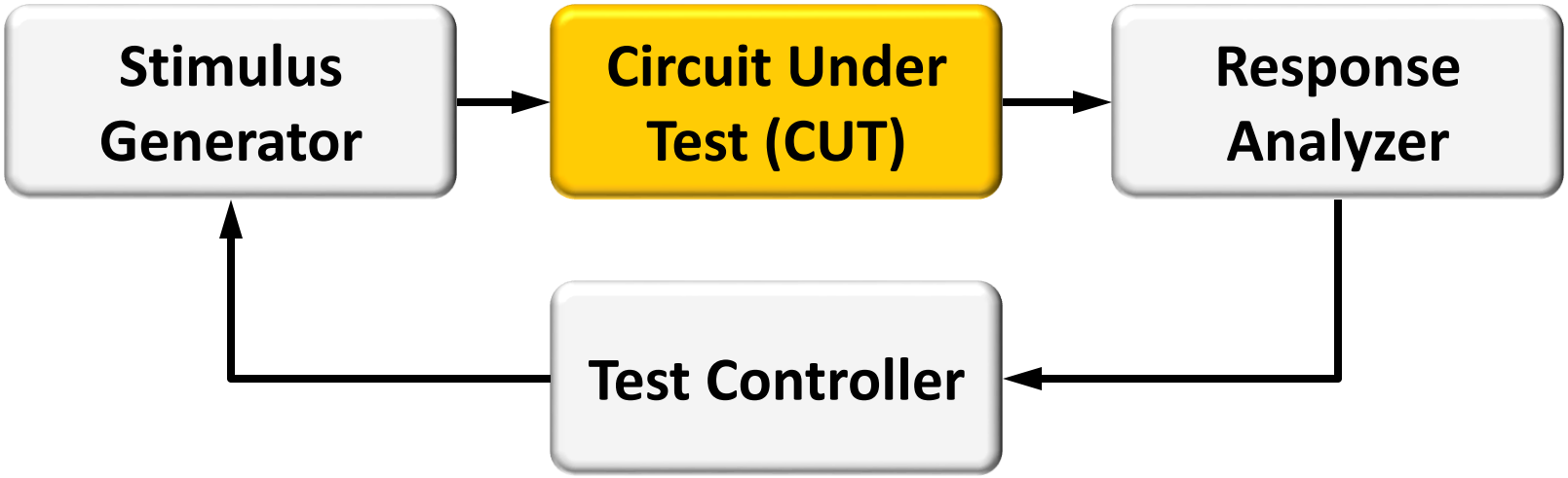
Single Clk

- No additional logic in the D→Q path, but o/p has extra load
- Scan operation results in dynamic nodes ⇒ need to be cautious of noise, and a minimum scan rate is necessary due to leakage
- Shift is destructive (=Load)

Clk must be **active** during scan

Self-Test

Becoming more important with increasing chip complexity and larger modules

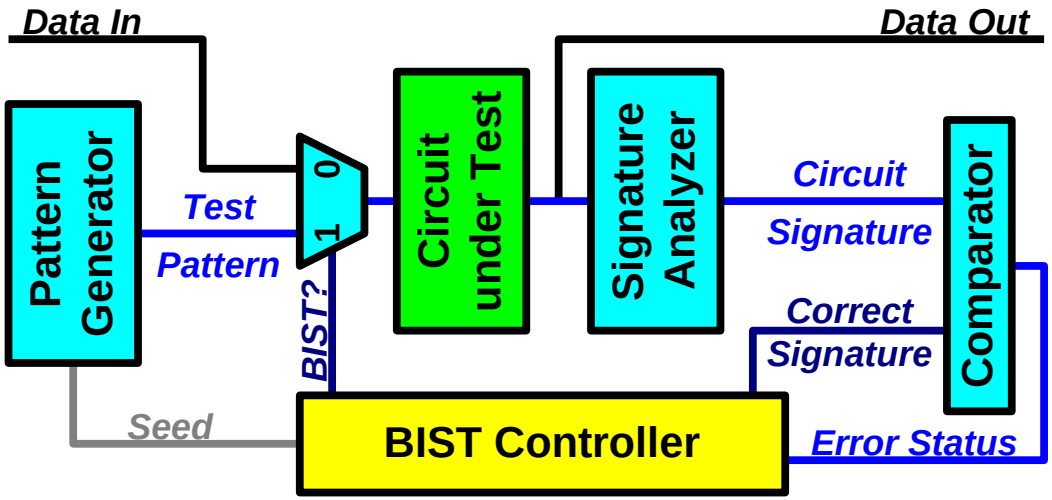


Built-In Self-Test (BIST)

- **The capability of a circuit to test itself**
  - Minimal external requirements (ck, si, so, control)

Pros	Cons
At-speed testing	Small area/delay penalty
Removes (or reduces) time and effort required for ATG	May be difficult for faults insensitive to random patterns (64-bit NOR)
Reduces tester time & ports, thereby saving $$$	Aliasing in output compression introduces risk in error detection
Independent of fault model	

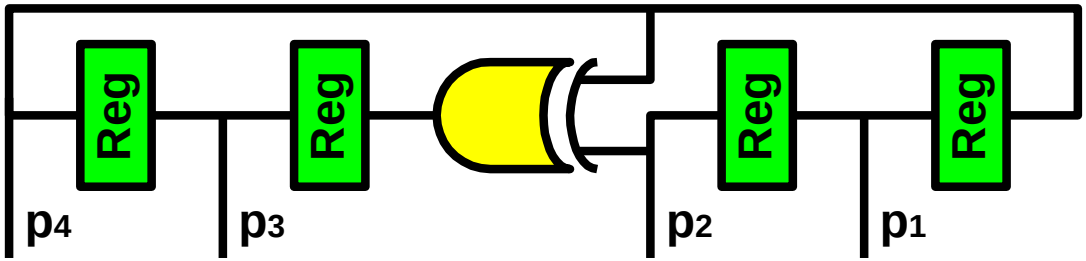
General BIST Architecture



- **Pattern generator may need to be initialized**
- **Error status could be as simple as pass/fail**

- **One BIST controller may govern multiple CUTs**
  - This interfaces to the tester
  - I/O to/from controller is serial to reduce wiring

4-bit LFSR as a Pattern Generator



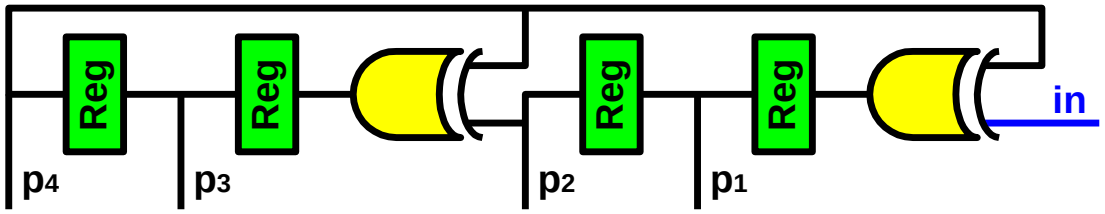
Characteristic Polynomial: X^4+X^2+1

- **All XOR functions can also be moved to the far RHS of LFSR**
  - Enables regularity in datapaths
  - Example on next slide
- **Easily incorporated into scan chain**

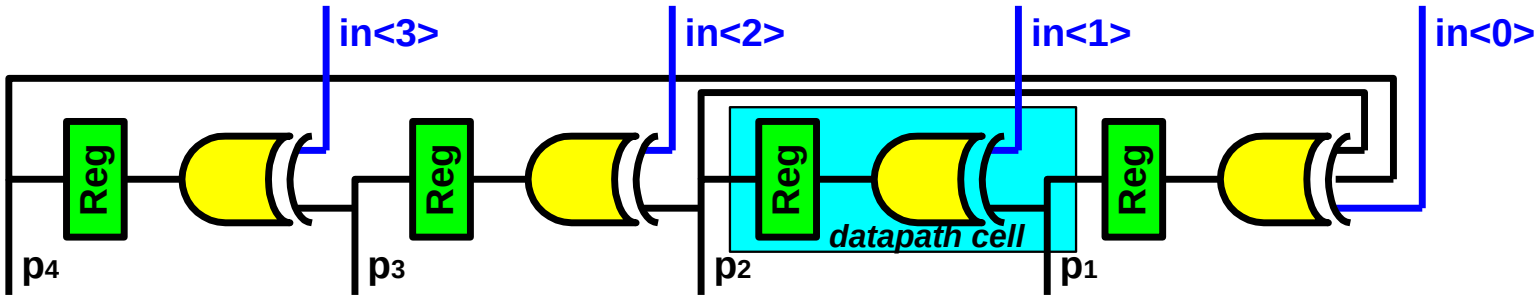
#	p4	p3	p2	p1
1	1	0	0	0
2	0	0	1	1
3	0	1	1	0
4	1	1	0	0
5	1	0	1	1
6	0	1	0	1
7	1	0	1	0
8	0	1	1	1
9	1	1	1	0
10	1	1	1	1
11	1	1	0	1
12	1	0	0	1
13	0	0	0	1
14	0	0	1	0
15	0	1	0	0

Signature Analyzers

- **One's counter:** n-bit counter x m-bit inputs
- **Transition counter:** n-bit counter x m-bit inputs
- **Single Input LFSR:** n-bit LFSR x m-bit inputs



- **Multiple input LFSR:** m-bit LFSR



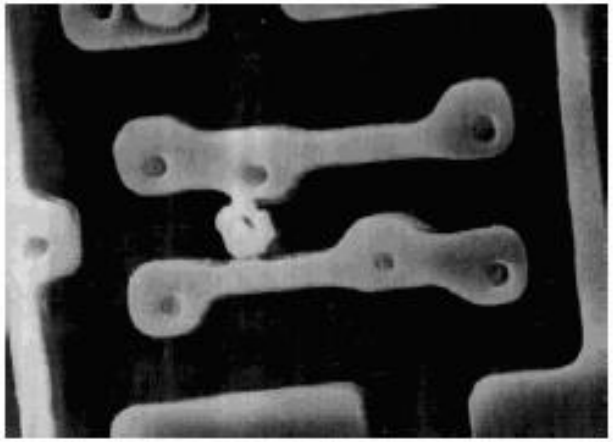
Spare Gates (a.k.a “Happy Gates”)

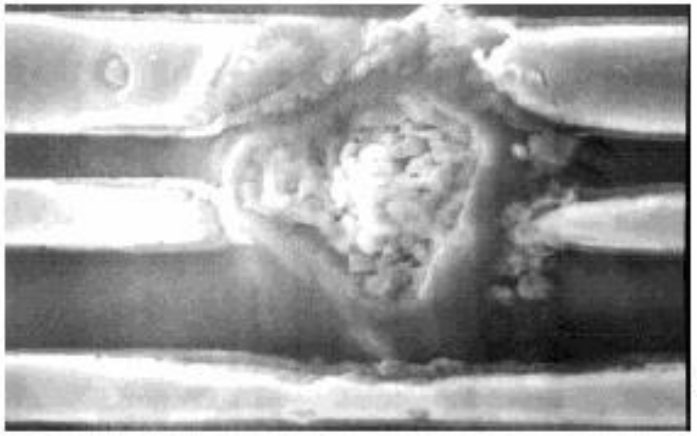
- **Post-silicon edits can be done using FIB**
  - Remove or add wires
- **FIB cannot add new devices, but**
  - Designers can throw some extra devices in the layout
  - Need to put them in the schematics too (LVS…)
- **Spare gates are basic cells with grounded inputs**
  - They don’t to anything normally (except take up space)
  - You can insert them using a FIB edit layer
  - Mixture of Inv, Nand, Nor, Flops…
  - Insert these in your blocks wherever you have room

Courtesy: M. Horowitz

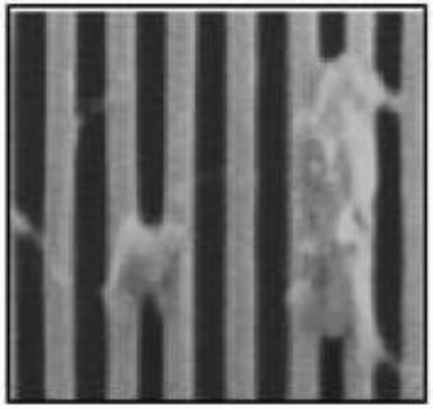
SEM Looks at Chips in a Vacuum

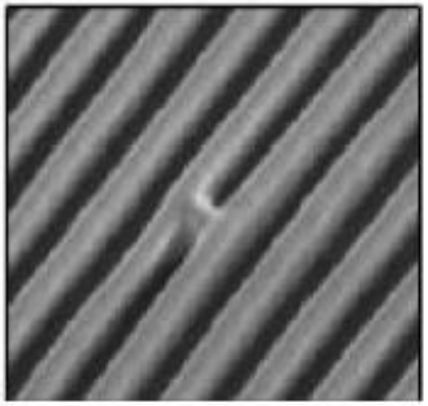
Useful for defect analysis



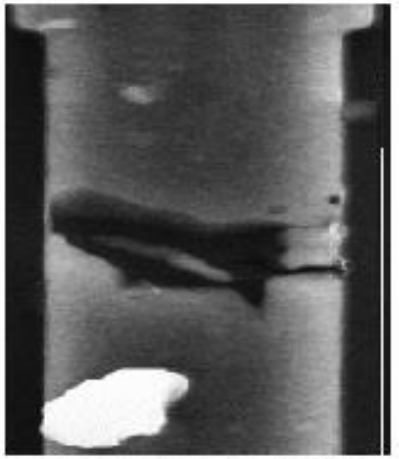


Source: M. Heath, Intel





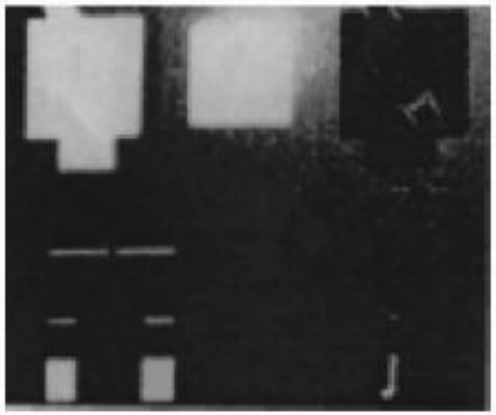
Source: KLA-Tencor



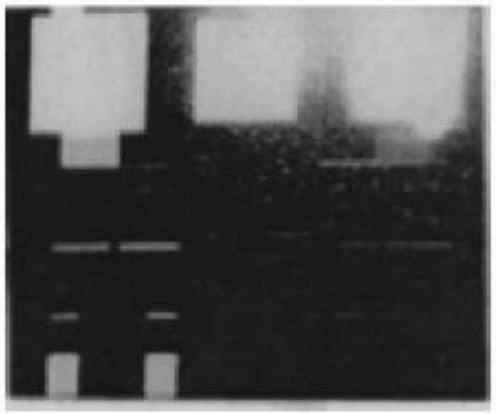
Source: ifw-dresden.de

E-beam Probing and Controlling

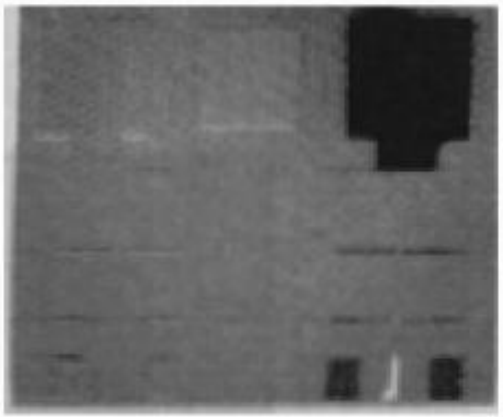
- **E-beam probing is a technique that requires face access**
  - Shoot e^- at the chip and measure reflected e^-
  - Gnd metals look bright; high-voltage metals look dark
  - Can probe metals this way to find out their voltages
  - Can pulse e-beams at higher energy to charge up nodes
    - Mild form of controllability to go along with observability



Potential contrast image of nondefective specimen



Potential contrast image of defective specimen

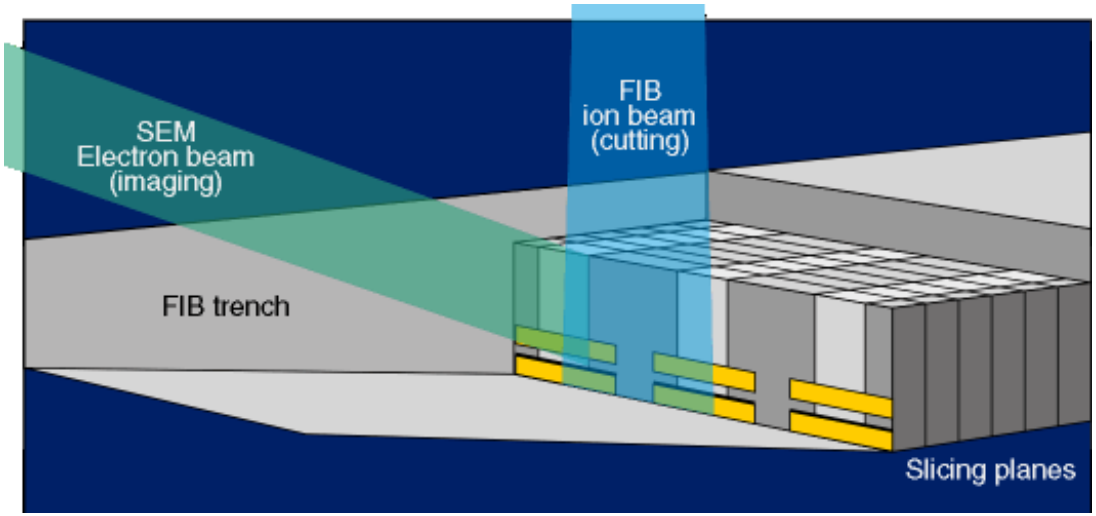


Differential image

Source: www.necel.com

Courtesy: M. Horowitz

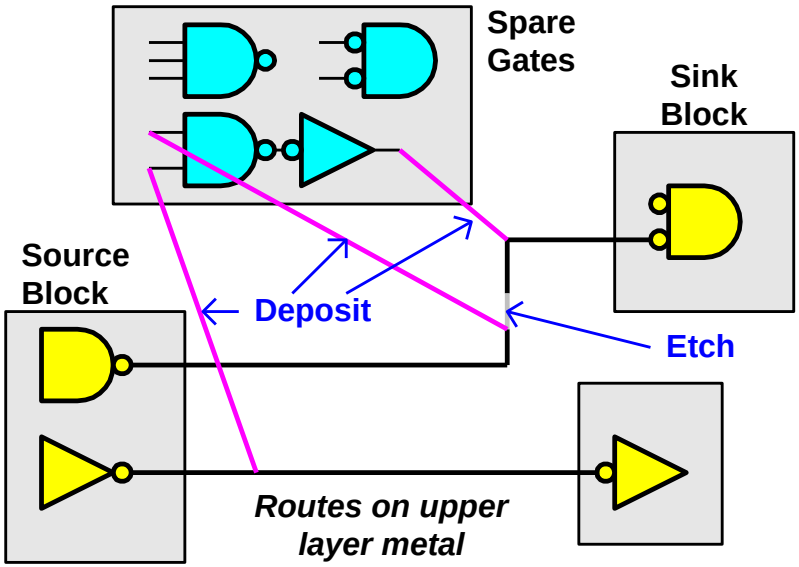
Focused Ion Beam (FIB) for Chip Edits



- **Allows post-fabrication edits on silicon**
  - Very expensive (~$400/hr)
    - Usually 3-5 hours per “normal” fix / one chip at a time
- **FIB edits can be additive or subtractive**
  - Cut wires or lay down new wires
- **FIB used to be from the top of the chip only**
  - Today can also be used for backside FIB (for flip-chip)

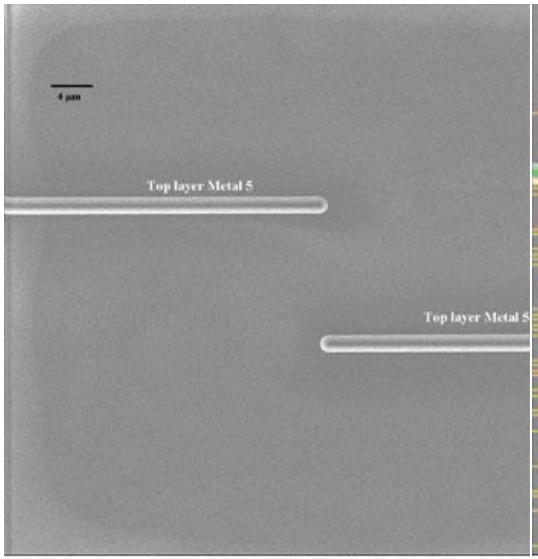
FIB Repair

- **Used to etch & deposit metals to make repairs**
  - **Example:** through your debug features, you believe the signal below needs to be AND'ed with another signal

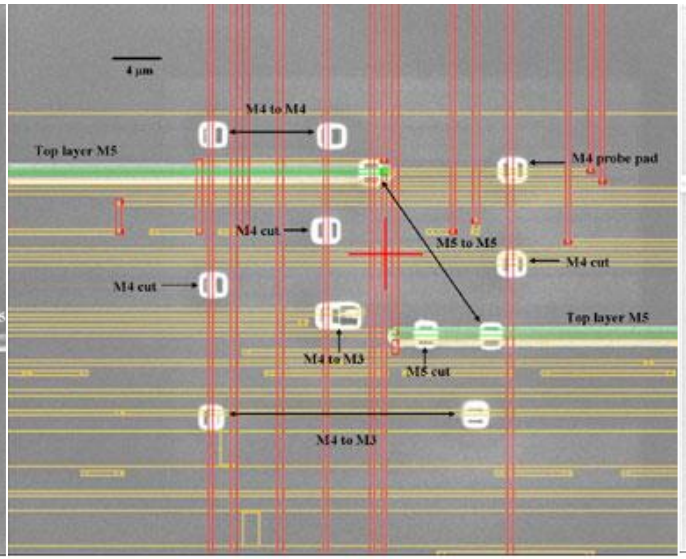


- Simulations seems to confirm this, but to be sure you'd like to try the repair on a real part to see if it truly fixes the bug
- **Spare gates need to be included in the design**

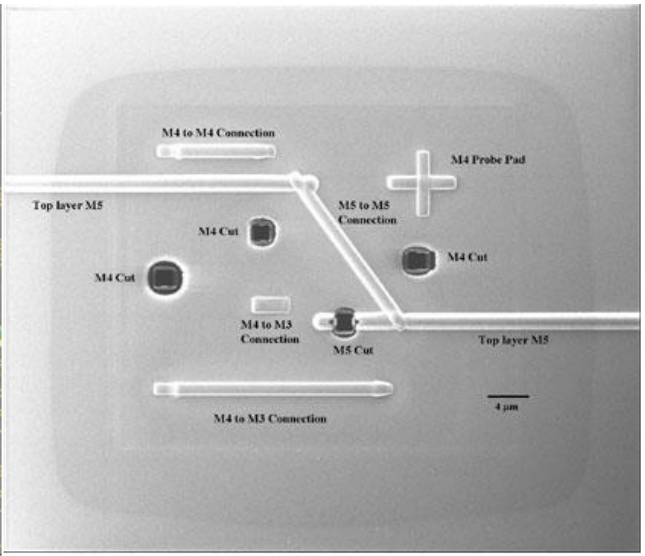
FIB Etch & Deposition Process



FIB Fig 1:
FIB image of a five layer device before any edits. Note tha layer metal is visible (Metal 5).



FIB Fig 2:
Same area as Fig.1 with CAD overlay superimposed and intend metal lines exposed.

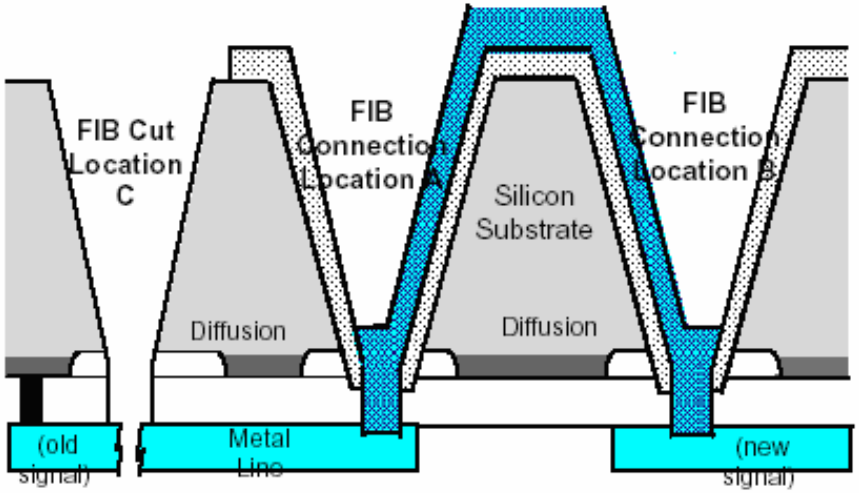


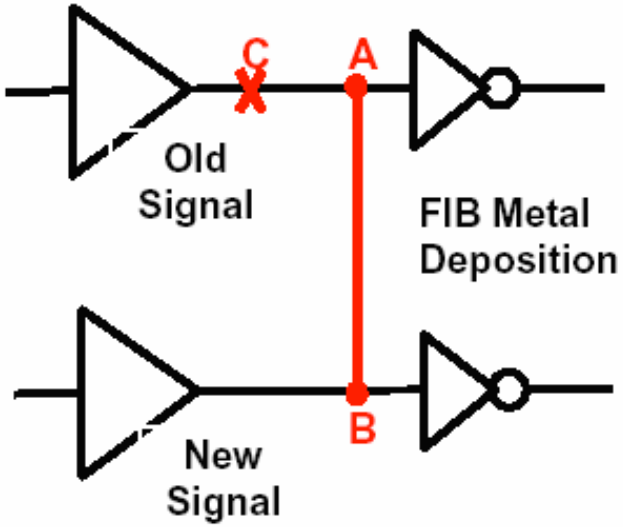
FIB Fig 3:
Same area as Fig.1 showing completed edits (interconnects, cuts, and a probing pad).

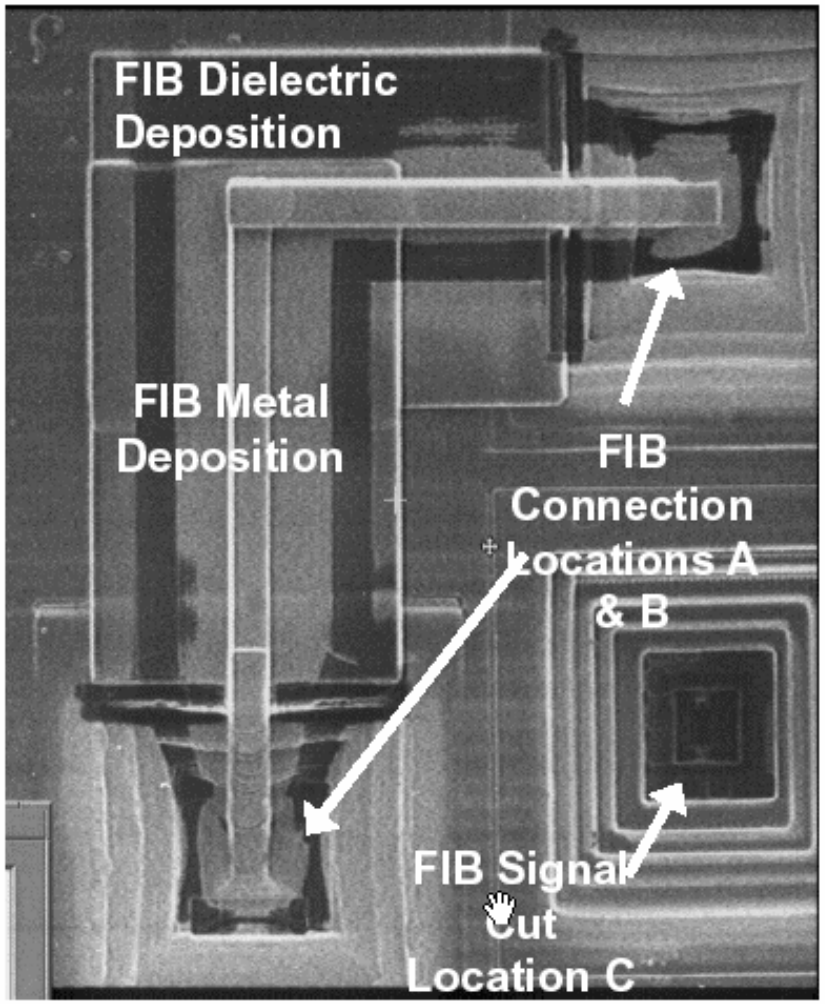
- **FIB image of metal lines to be connected**
- **CAD overlay to identify locations of etch & deposition**
- **Final view of repair after FIB with chemical gases**

Images courtesy of Accurel

FIB Example

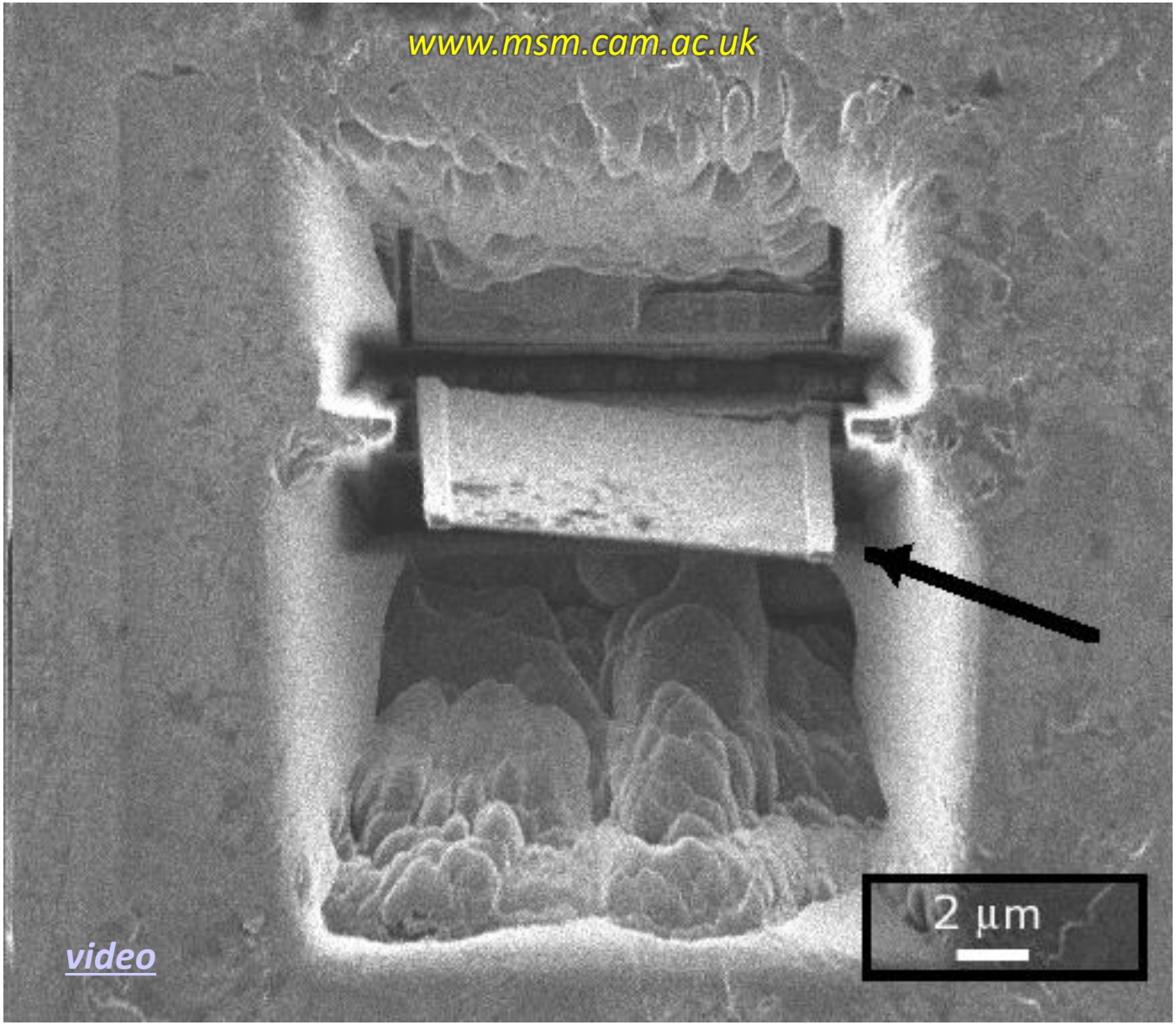






Source: Stinson, Intel

Another FIB Example



Summary

- **Wide high-level metal lines for power and ground**
- **Several decades of decoupling capacitance**
  - At least 10x more than switched cap
- **Scaling makes chips more difficult to test and debug**
- **Scan chains are practically a must**
- **Make smart use of “happy gates” and BIST**