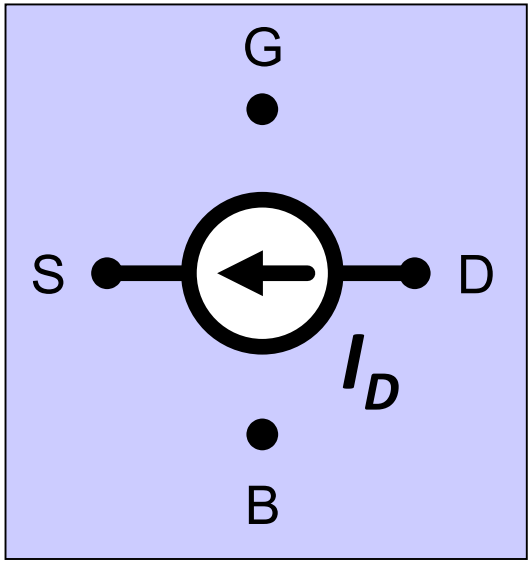
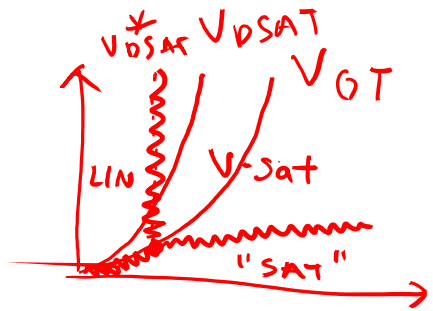
ECE115C – Digital Electronic Circuits

Lecture 3:
MOS RC Model, CMOS Manufacturing

Lecture 2 Summary: MOS I-V Model

$$V_{GT} = V_{GS} - V_T$$





Subthreshold region ($V_{GT} \leq 0$)

$$I_D = I_0' \cdot \frac{W}{W_0} \cdot 10^{\frac{V_{GS} - V_T + \gamma_D \cdot V_{DS}}{S}}$$

Active region ($V_{GT} \geq 0$) Lin, Sat, V-Sat

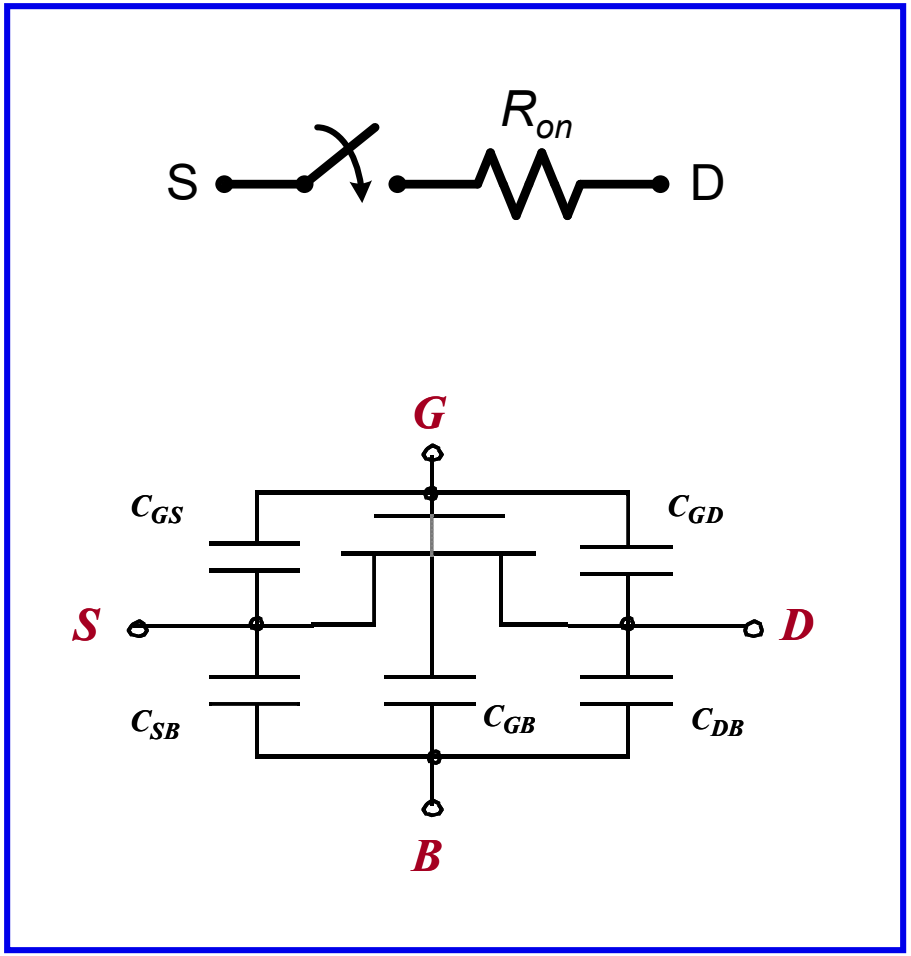
$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2}\right) \cdot (1 + \lambda \cdot V_{DS})$$

$$V_{min} = min(V_{DS}, V_{GT}, V_{DSAT}^*)$$

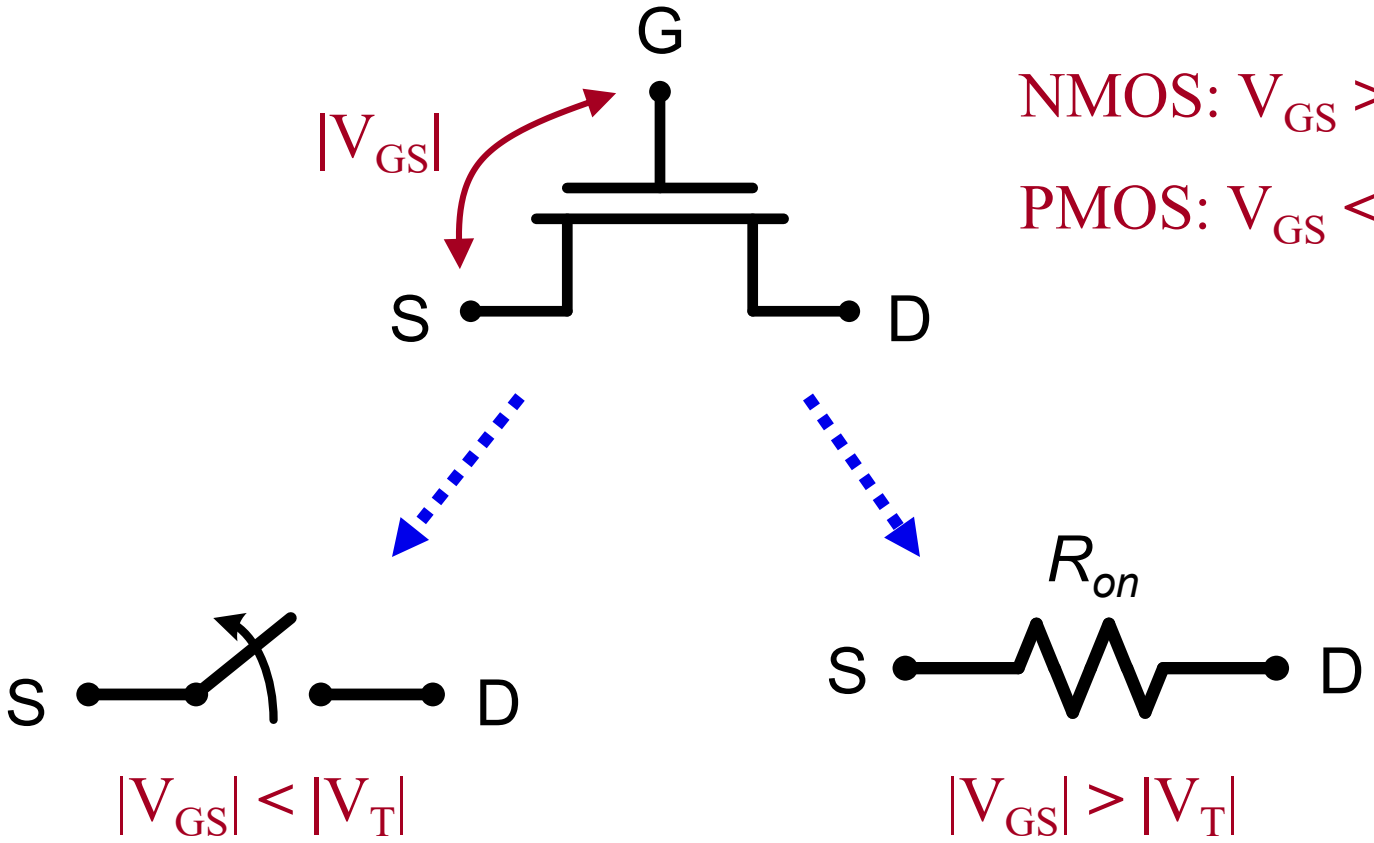
Lin Sat V-Sat

Agenda

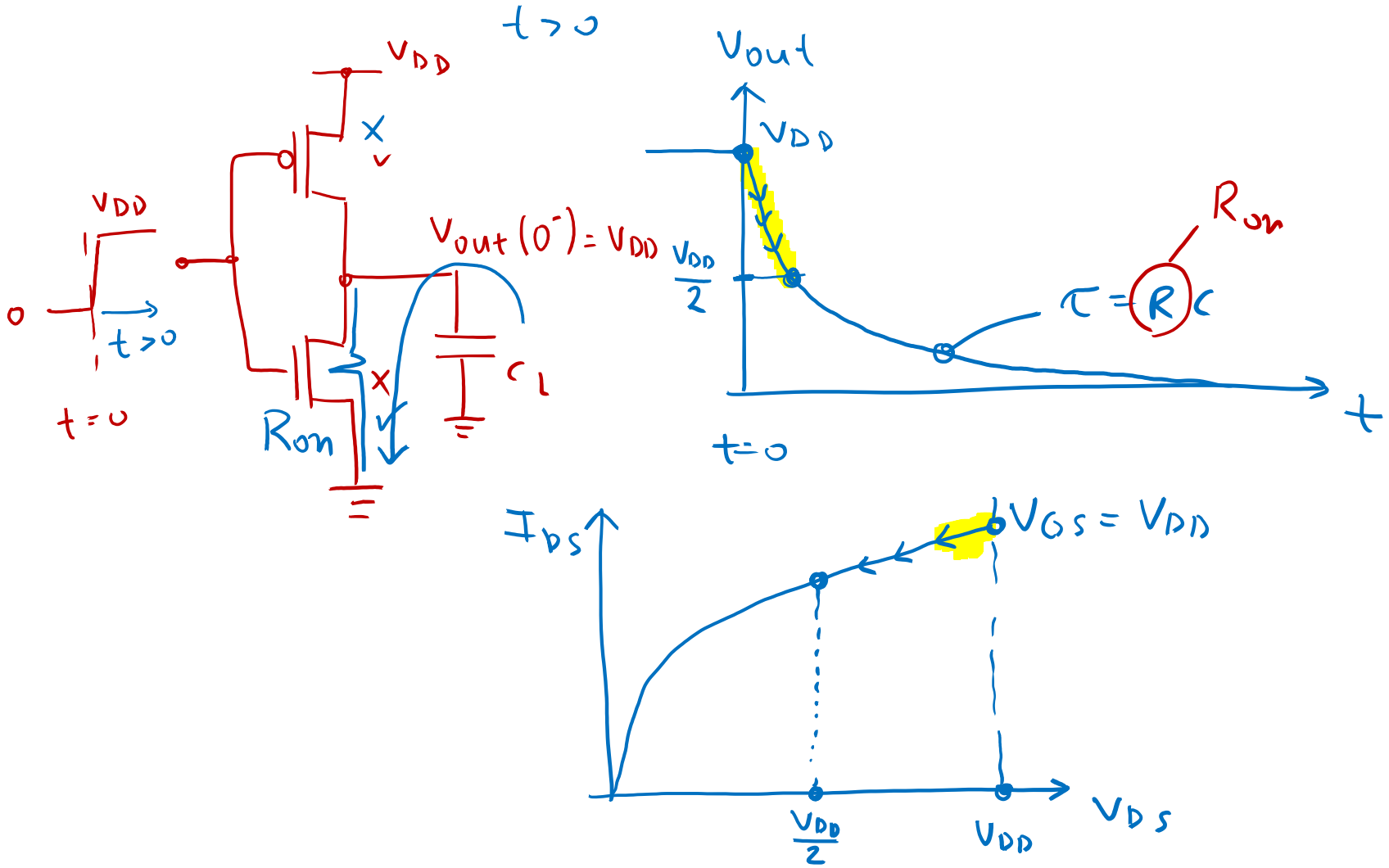
- **MOS Transistor: RC Model** (pp. 104-113)
- CMOS Manufacturing Process (pp. 36-46)



Switch Model of CMOS Transistor



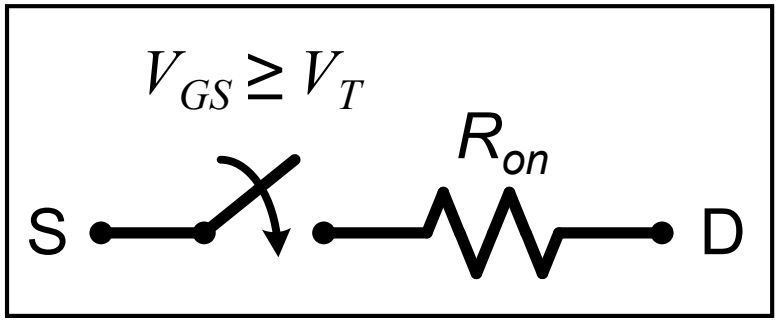
Switching Behavior



The Transistor as a Switch

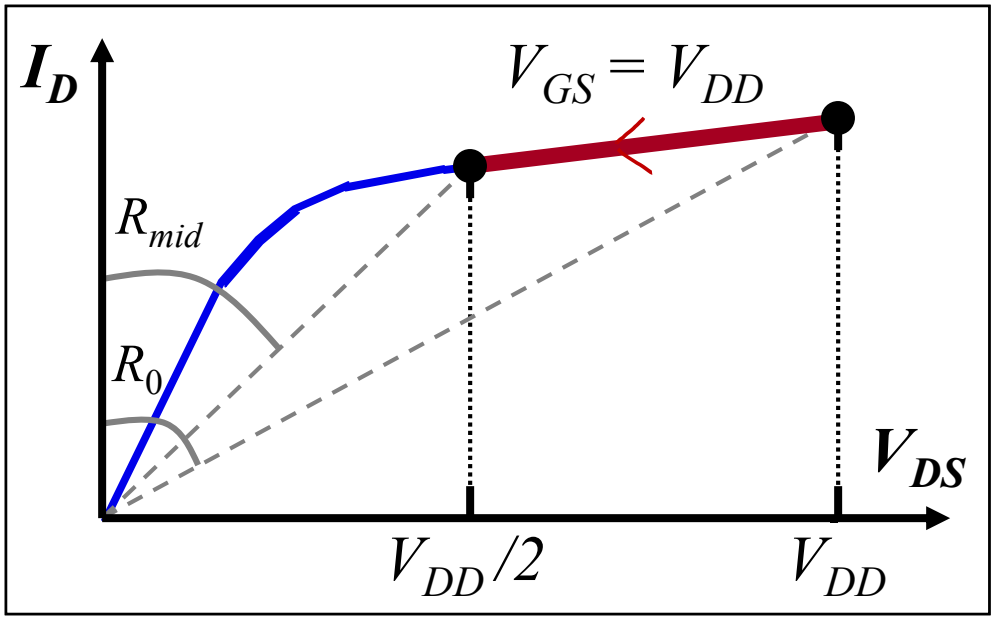
- **MOS can be treated as equivalent resistance**

Calculating MOS resistance: $$R(V_{DS}) = \frac{V_{DS}}{I_{DSAT} \cdot (1 + \lambda V_{DS})}$$



$$R_{on} \approx \frac{1}{2}(R_0 + R_{mid})$$

good approximation (I-V ≈ linear)



- **This model will be used for delay analysis**

Computing Equivalent Resistance (1/2)

- **Method 1 ("exact"): by integration**

$$R_{on} = \frac{1}{-V_{DD}/2}\int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}\cdot(1+\lambda V)}dV \ldots \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

$$k'\frac{W}{L}\left[(V_{DD}-V_T)V_{DSAT}-\frac{V_{DSAT}^2}{2}\right]$$

V_{GS}

$$\boxed{R_{on} \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)}$$

Computing Equivalent Resistance (2/2)

- **Method 2: simple averaging**
  - The averaging works because of approximately linear dependence of I_{DS} on V_{DS} (recall the CLM model)

$$R_{on} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}\cdot(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}\cdot(1+\lambda V_{DD}/2)}\right)$$

R_0 $\qquad$ R_{mid}

$$k'\frac{W}{L}\left[(V_{DD}-V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$$

V_{GS}

fixed L
$\Rightarrow R_{on} \sim \frac{1}{W}$

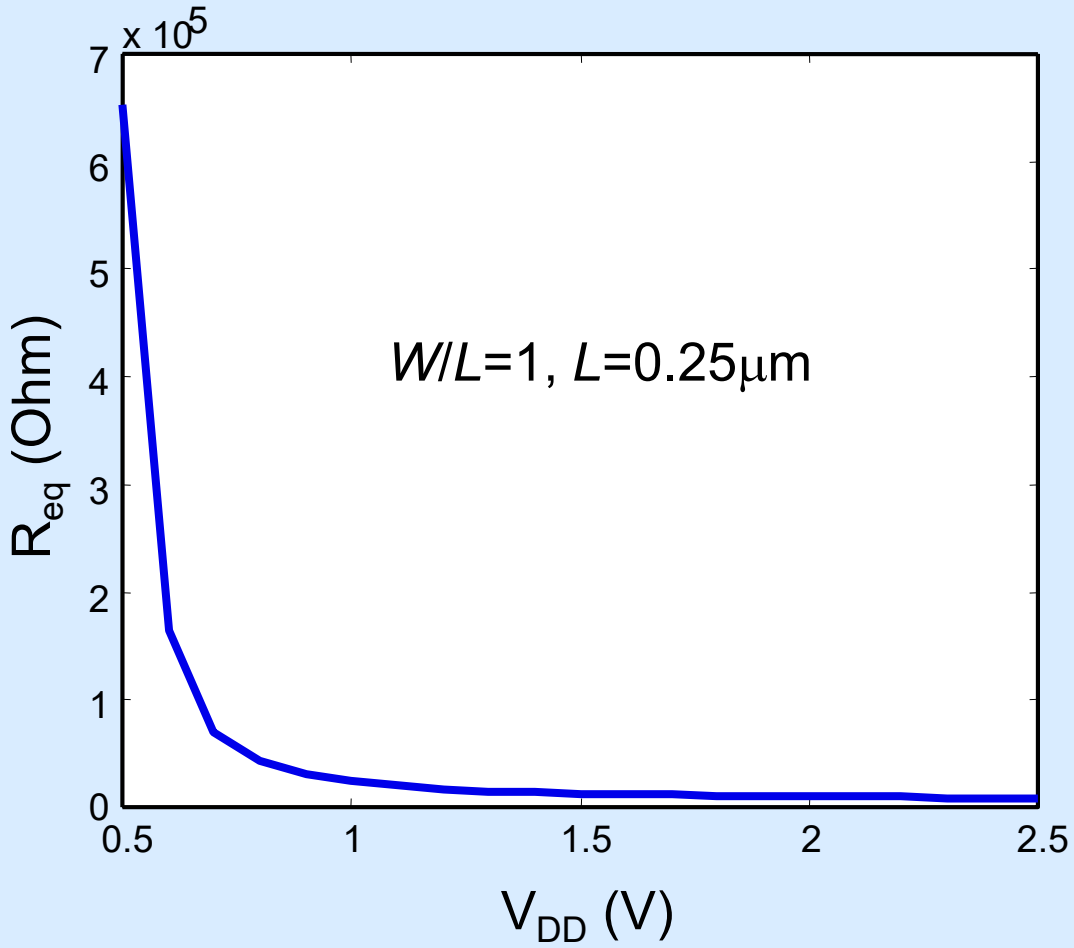
$R_{on} \sim \frac{L}{W}$

$$R_{on} \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

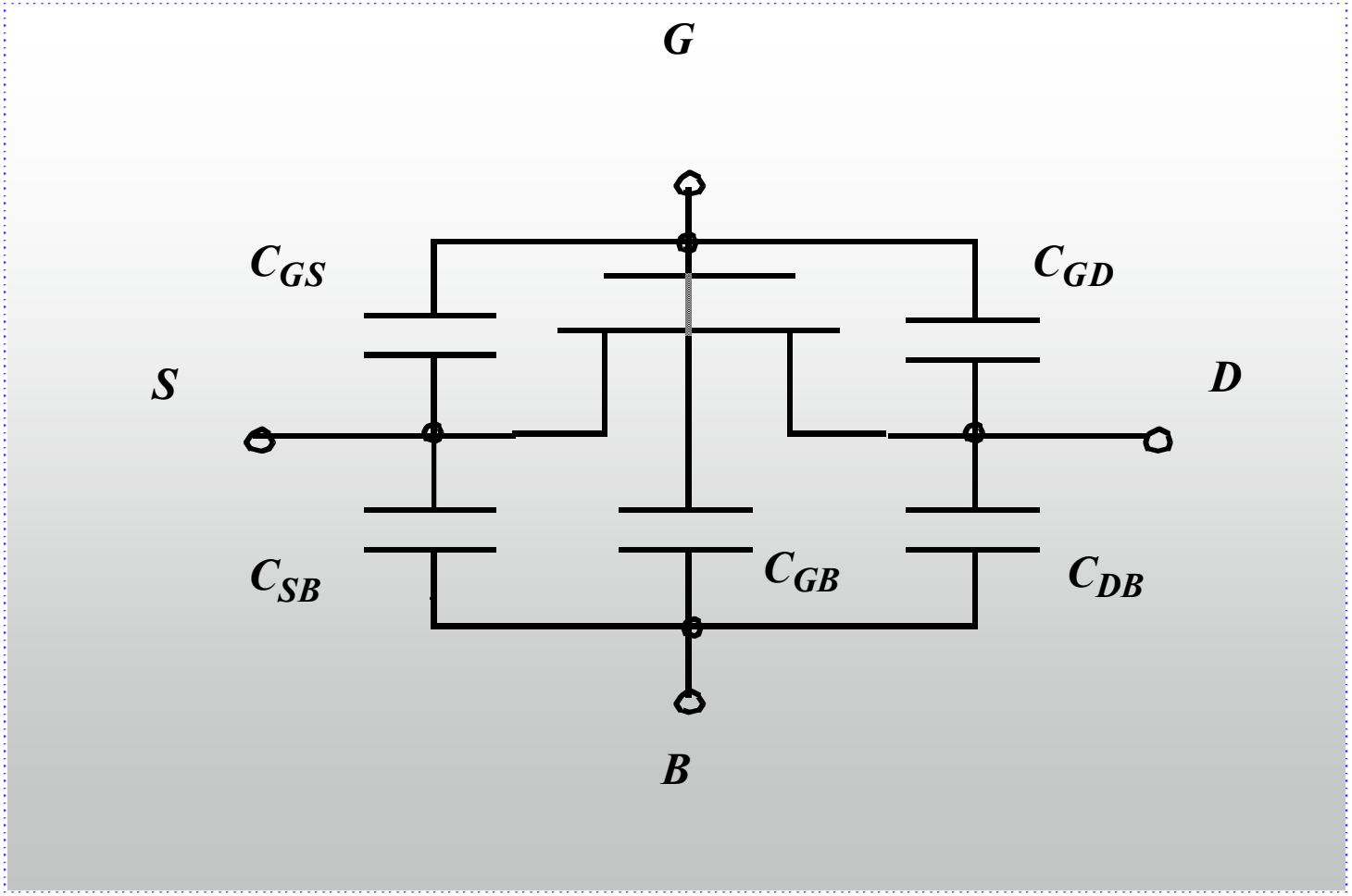
Use this formula for hand analysis

R_{on} vs. V_{DD} (Simulation Result)

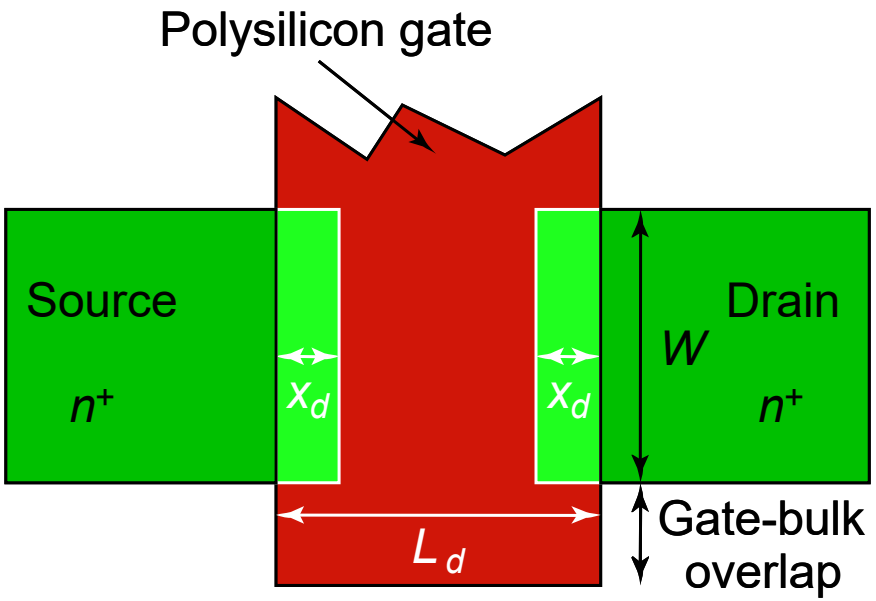
- R_{on} increases rapidly as V_{DD} approaches V_T



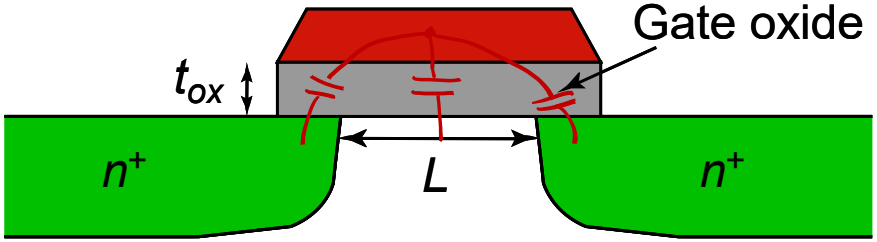
MOS Capacitances



The Gate Capacitance

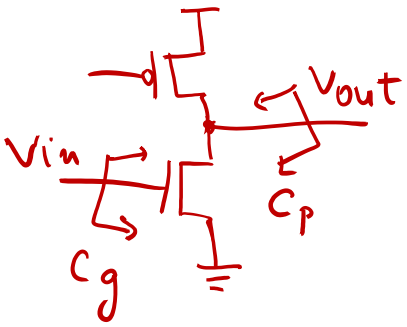


Top view



Cross section

$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$



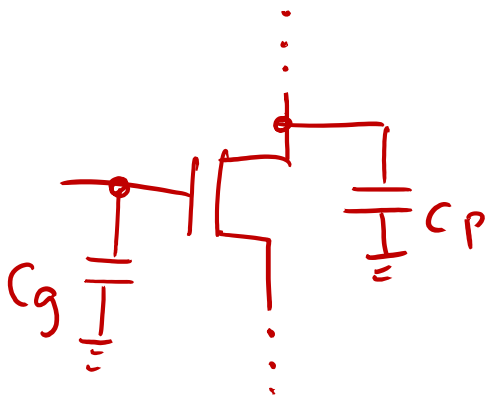
Capacitance Components

- #1: Gate-Channel Capacitance
- #2: Gate Overlap Capacitance

} C_g

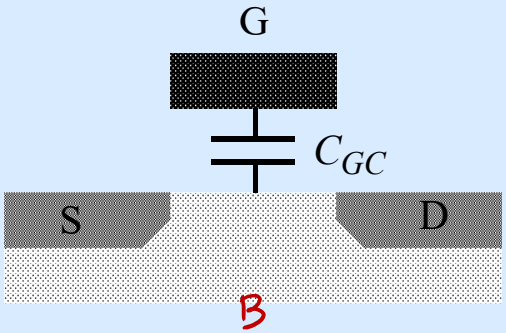
- #3: Junction/Diffusion Capacitance

} S/D C_P

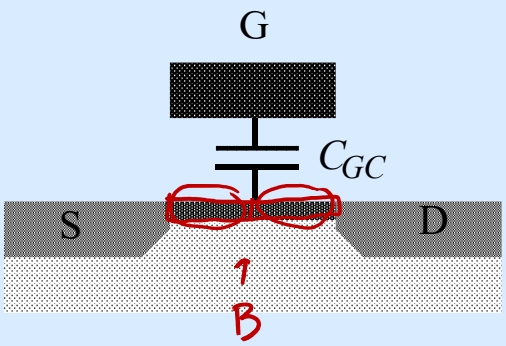


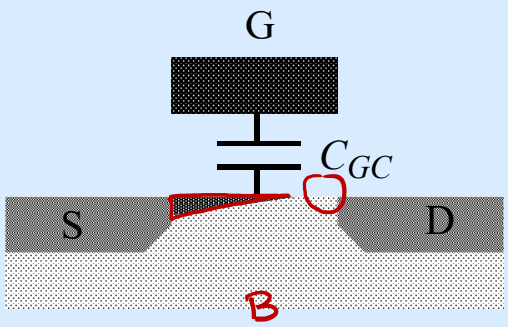
#1: Gate-Channel Capacitance

$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$



Cut-off

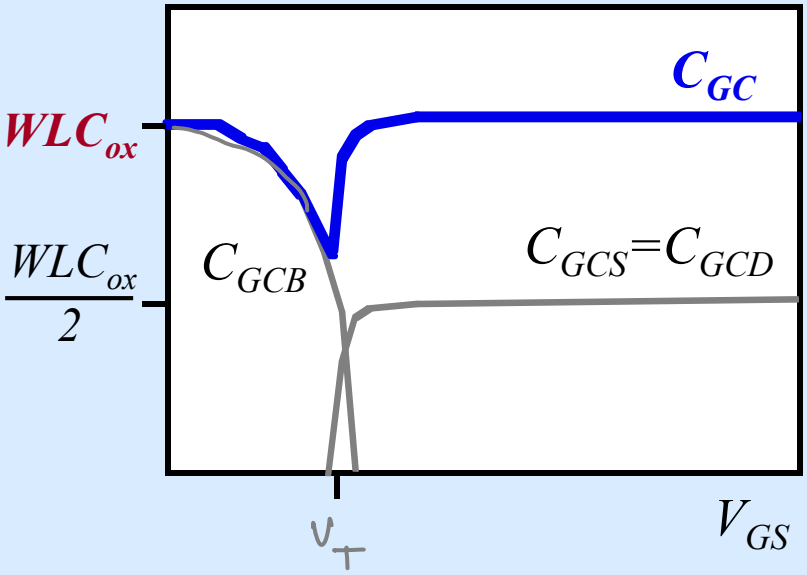




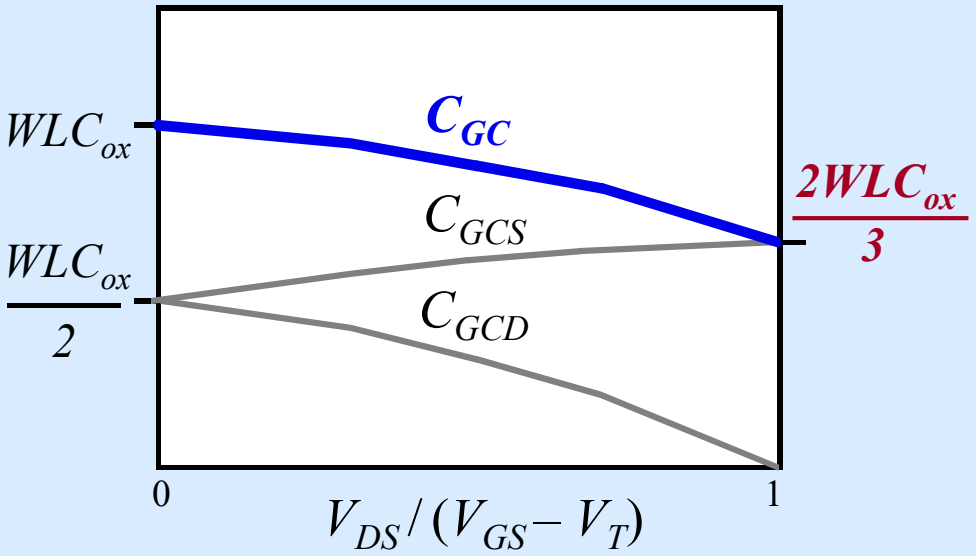
Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

A Close Look at Gate-Channel Capacitance

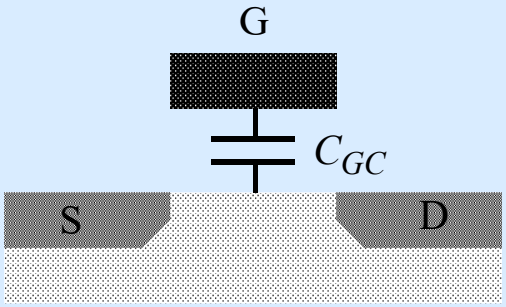


C_{gate} as a function of V_{GS} (with V_{DS} = 0)

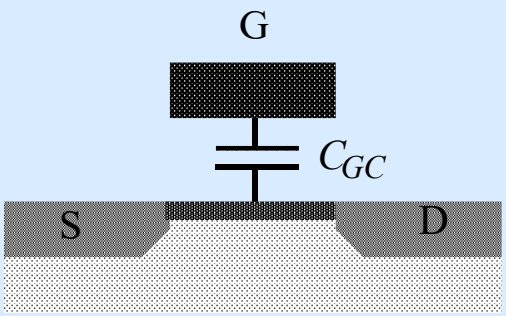


C_{gate} as a function of the degree of saturation

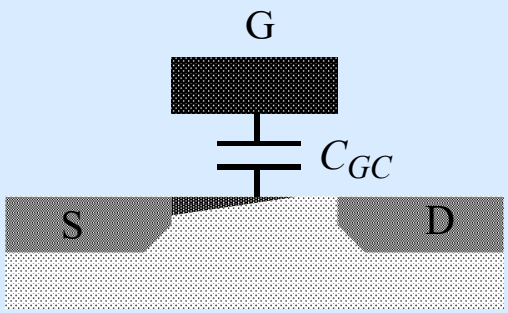
Summary: #1: Gate-Channel Capacitance



Cut-off



Resistive



Saturation

Operation Region	C_{GCB}	C_{GCS}	C_{GCD}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Textbook: page 109

Off/Lin → $C_{gate} = C_{ox} \cdot W \cdot L_{eff}$

Sat → $C_{gate} = (2/3) \cdot C_{ox} \cdot W \cdot L_{eff}$

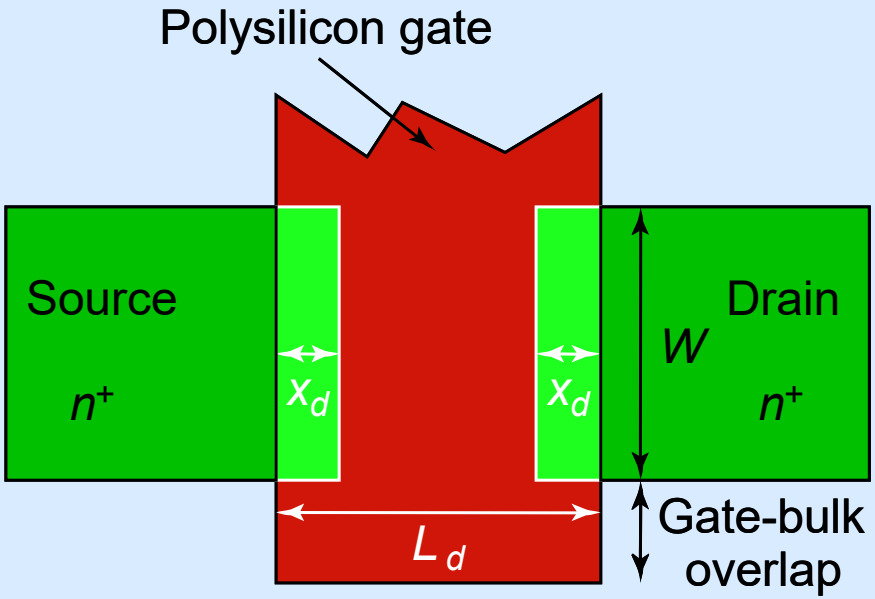
$C_g \sim W$

$L_d = 120\,nm$
$x_d = 15\,nm$
$\rightarrow L_{eff} = 0.09\,\mu$
$W = 0.24\,\mu m$

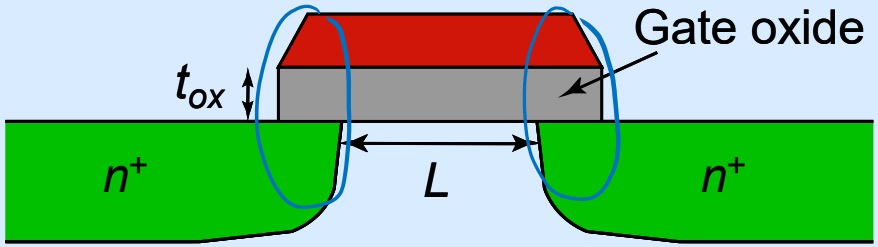
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \approx 15\,\frac{fF}{\mu m}$$

$15\,fF/\mu m^2 \times 0.24 \times 0.09 = 0.2\,fF$

#2: Gate Overlap Capacitance



Top view



Cross section

15 0.015

$$C_O = C_{ox} \cdot x_d$$

0.225

e.g. 0.24μ

Off/Lin/Sat → $C_{GSO} = C_{GDO} = C_O \cdot W$ → 0.05fF

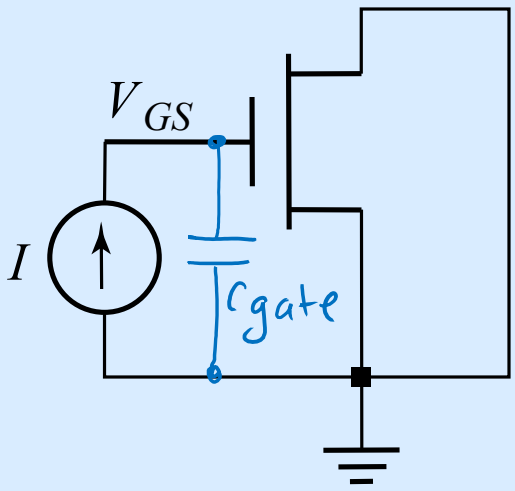
S+D overlap

$C_g = C_{Gc} + C_o = 0.2\text{fF} + 0.05\times 2 = 0.3\text{fF}$

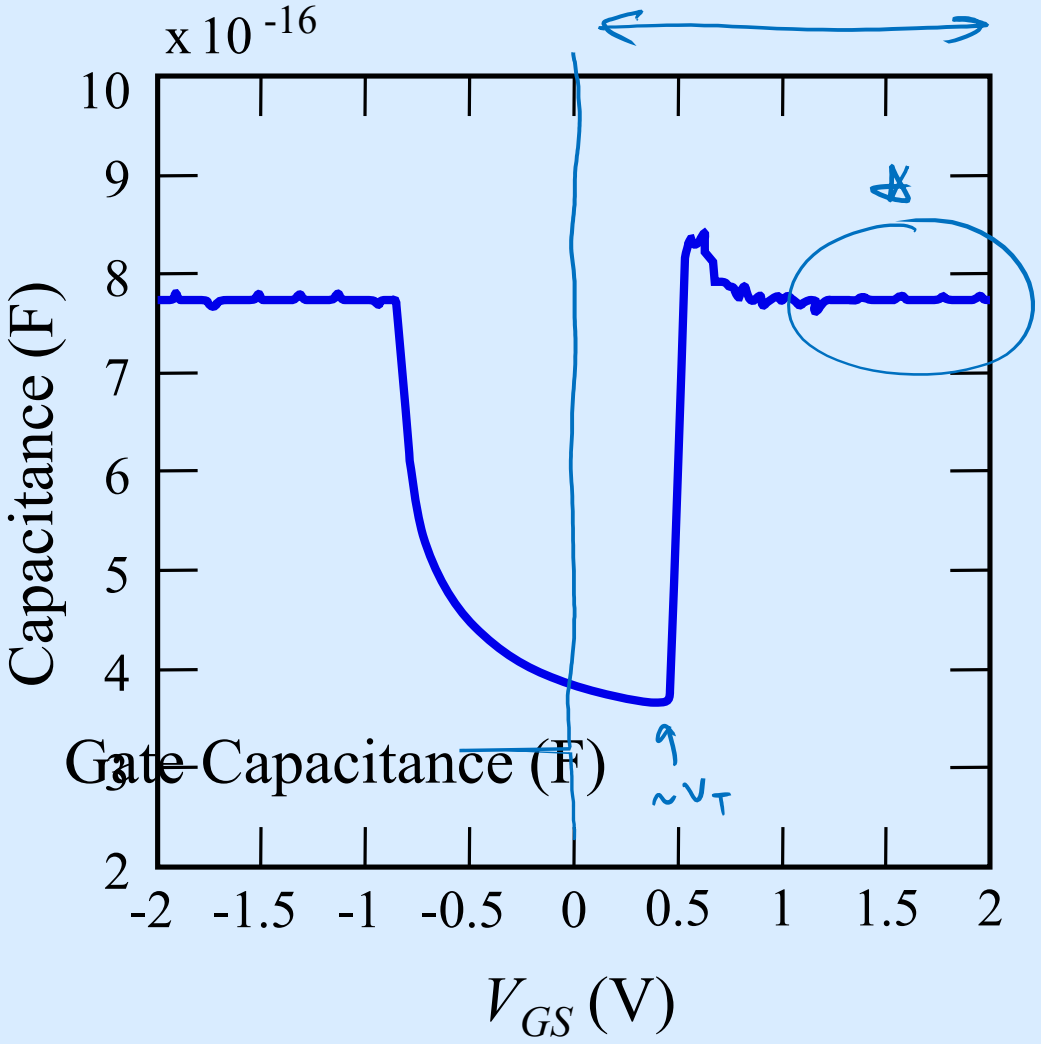
(prev. slide)

Measuring the Gate Cap

Transient analysis

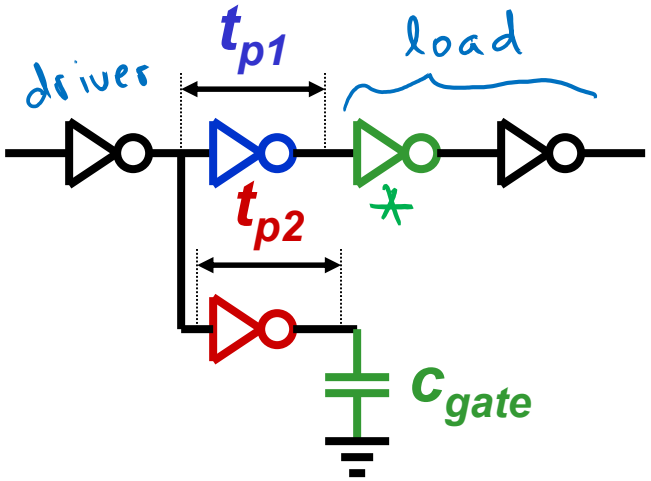


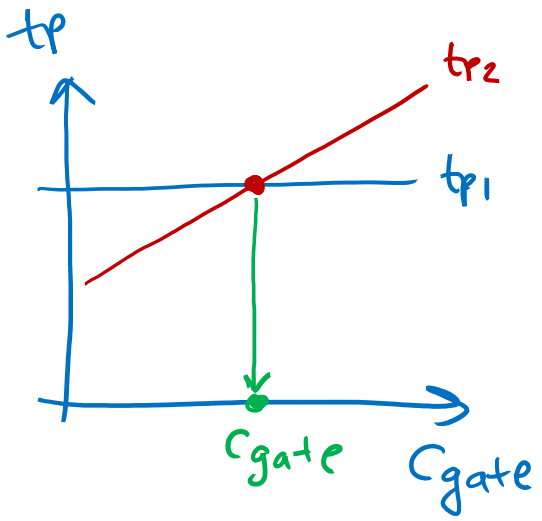
$$C_{gate} = \frac{I \cdot \Delta t}{\Delta V}$$



Finding Equivalent Capacitance – Delay

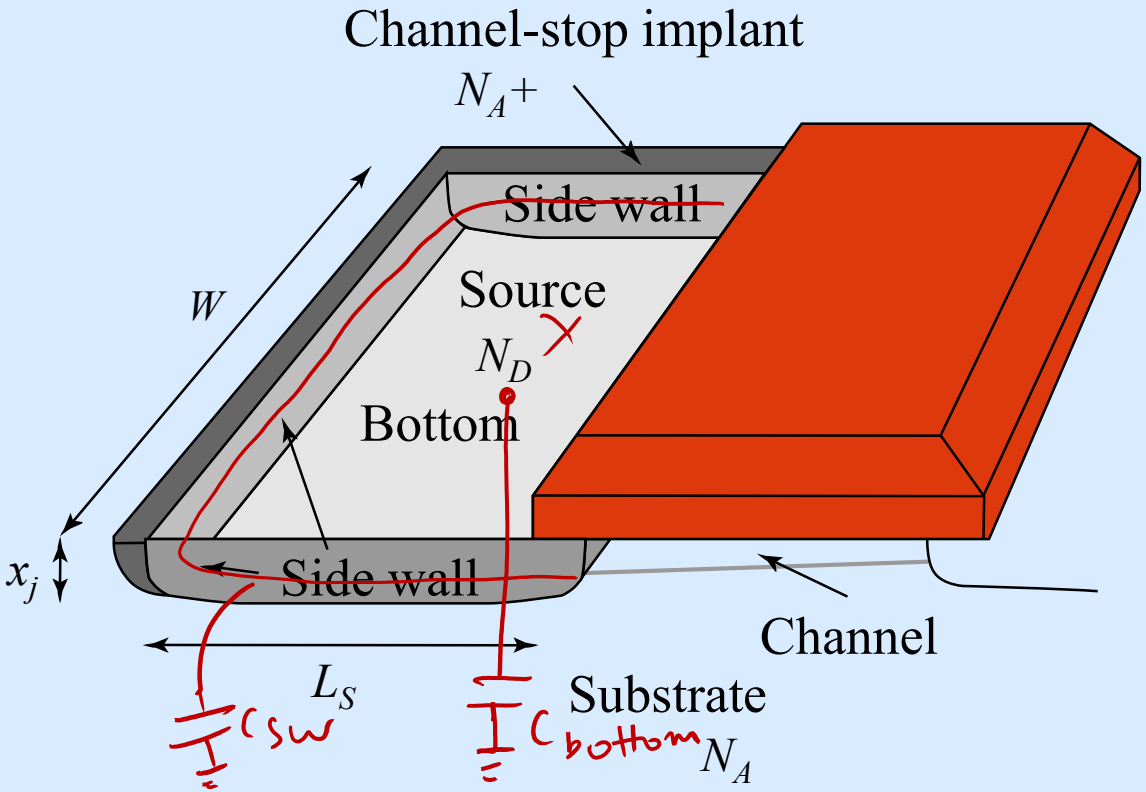
- Curve fitting approach to find a number that works for hand analysis of the gate delay
- Understand the limitations: the model will depend on signal rise times, voltage, temperature, process parameter variation





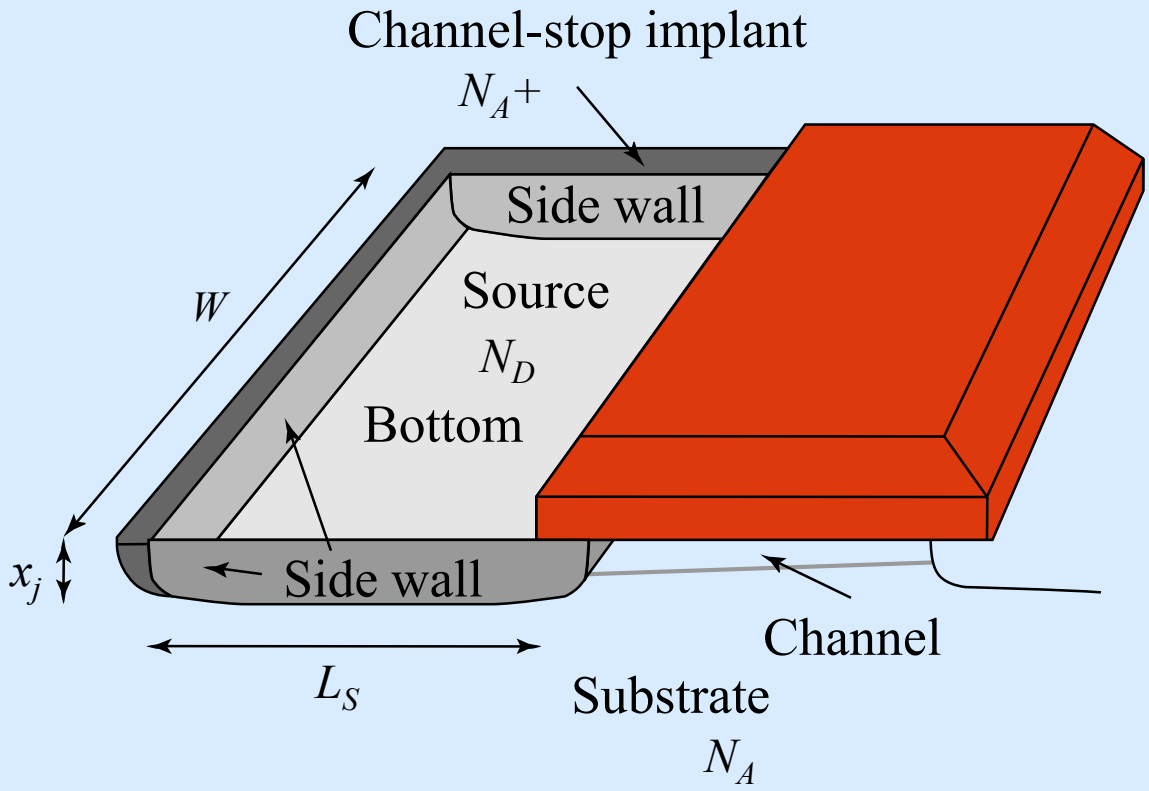
- Experiment: find C_{gate} to match propagation delays
  - $t_{p1} = t_{p2}$ → C_{gate} is equivalent cap of the green gate

#3: Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw}$$
$$= C_j \cdot AREA + C_{jsw} \cdot PERIMETER$$
$$= C_j (L_S W) + C_{jsw}(2L_S + W)$$

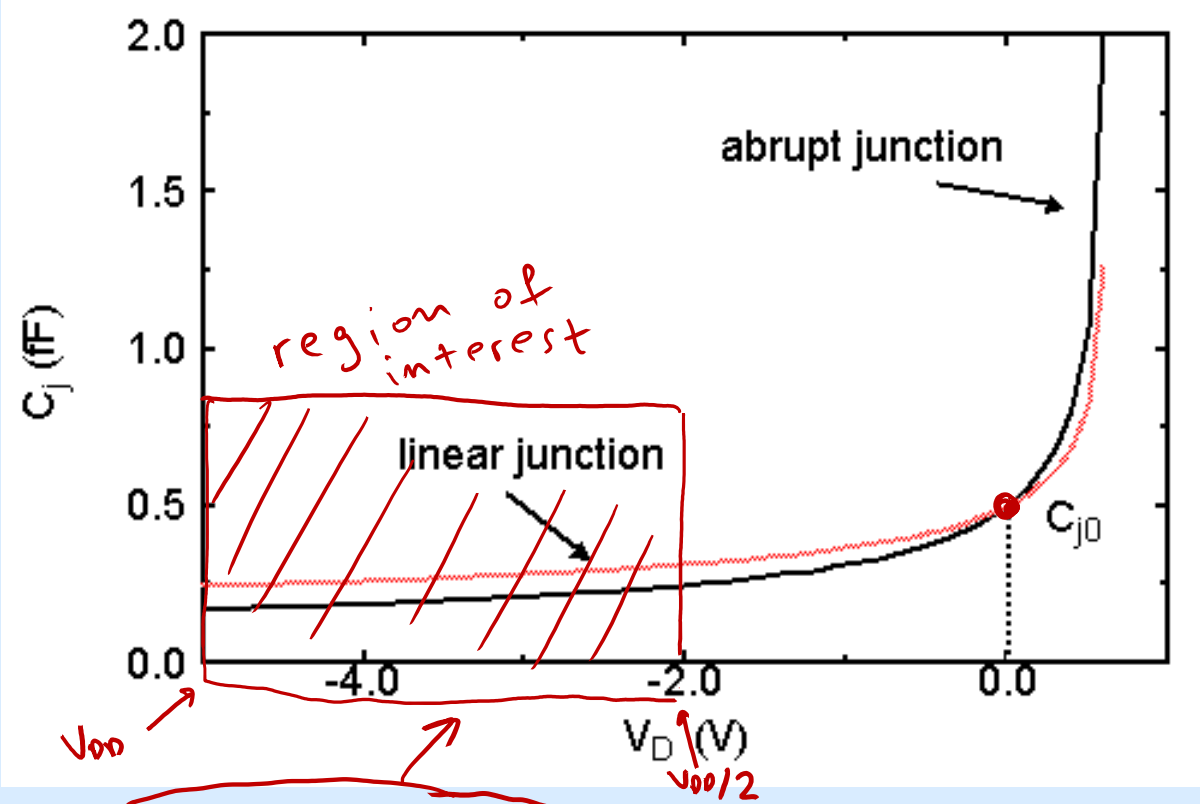
#3: Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw}$$
$$= C_j \cdot AREA + C_{jsw} \cdot PERIMETER$$

Off/Lin/Sat → $C_{diff} = C_j \cdot L_S \cdot W + C_{jsw} \cdot (2L_S + W)$

Junction Capacitance is Bias-dependent



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction

m = 0.33: linear junction

#3 Diffusion Capacitance: Summary of Equations

- **Bottom-plate C**

$$C_j = \frac{C_{j0}}{(1 - V_D/\Phi_0)^{m_j}}$$

C_{j0}: 0.8 fF/μm²; Φ_0: 0.8V; m_j: 0.22; C_j = 0.7 fF/μm²

m = 0.5: abrupt junction

m = 0.33: linear junction

- **Side-wall C**

$$C_{jsw} = \frac{C_{jsw0}}{(1 - V_D/\Phi_{0sw})^{m_{jsw}}}$$

C_{jsw0}: 0.05 fF/μm; Φ_{0sw}: 0.8; m_{jsw}: 0.01; C_{jsw} = 0.05 fF/μm²

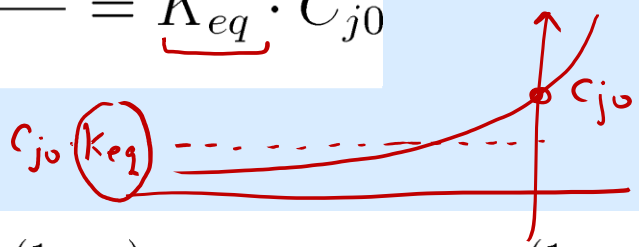
$$C_{diff} = C_j \cdot W \cdot L_S + C_{jsw} \cdot (2L_S + W) \ldots$$

linearize

Linearizing the Junction Cap

- Replace non-linear capacitance by large-signal equivalent linear capacitance, which displaces equal charge over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} \cdot C_{j0}$$



$$K_{eq} = \frac{-\Phi_0^m}{(V_{high} - V_{low}) \cdot (1-m)} \left[(\Phi_0 - V_{high})^{(1-m)} - (\Phi_0 - V_{low})^{(1-m)} \right]$$

Typical value for K_{eq} around 0.5

Summary: Capacitive Device Model

- Gate-Channel Capacitance
  - $C_{GC} = C_{ox} \cdot W \cdot L_{eff}$ (Off, Linear)
  - $C_{GC} = (2/3) \cdot C_{ox} \cdot W \cdot L_{eff}$ (Saturation)
- Gate Overlap Capacitance
  - $C_{GSO} = C_{GDO} = C_O \cdot W$ (Always)
- Junction/Diffusion Capacitance
  - $C_{diff} = C_j \cdot L_S \cdot W + C_{jsw} \cdot (2L_S + W)$ (Always)

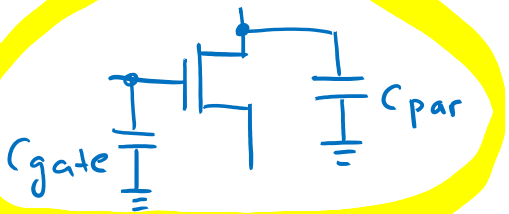
Zero-bias → $C_{diff} > C_{gate}$

MOS On → $C_{diff} \leq C_{gate}$

Circuit design

C_{gate}

$\approx 2\,fF/\mu m$



$C_{parasitic}$

$\approx 1.5\,fF/\mu m$

$$\gamma = \frac{C_{par}}{C_{gate}} = 0.75$$

technology dependent

Outline

- MOS Transistor: RC Model (pp. 104-113)
- **CMOS Manufacturing Process (pp. 36-46)**

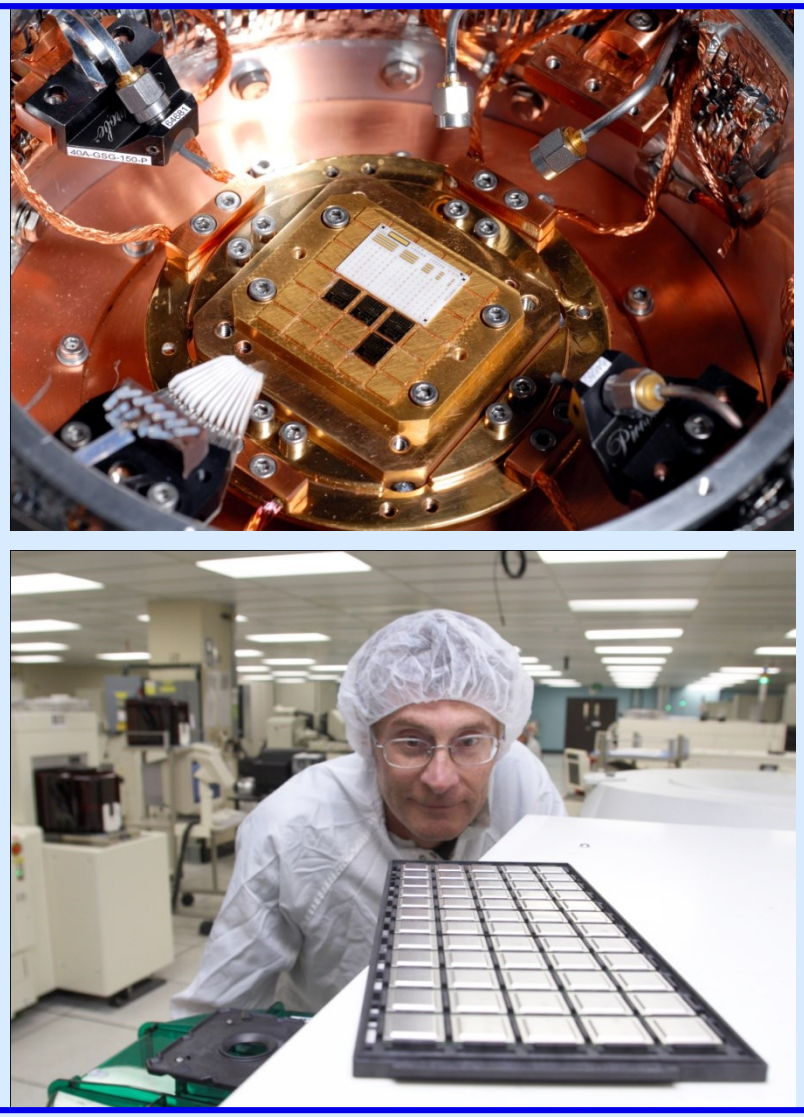
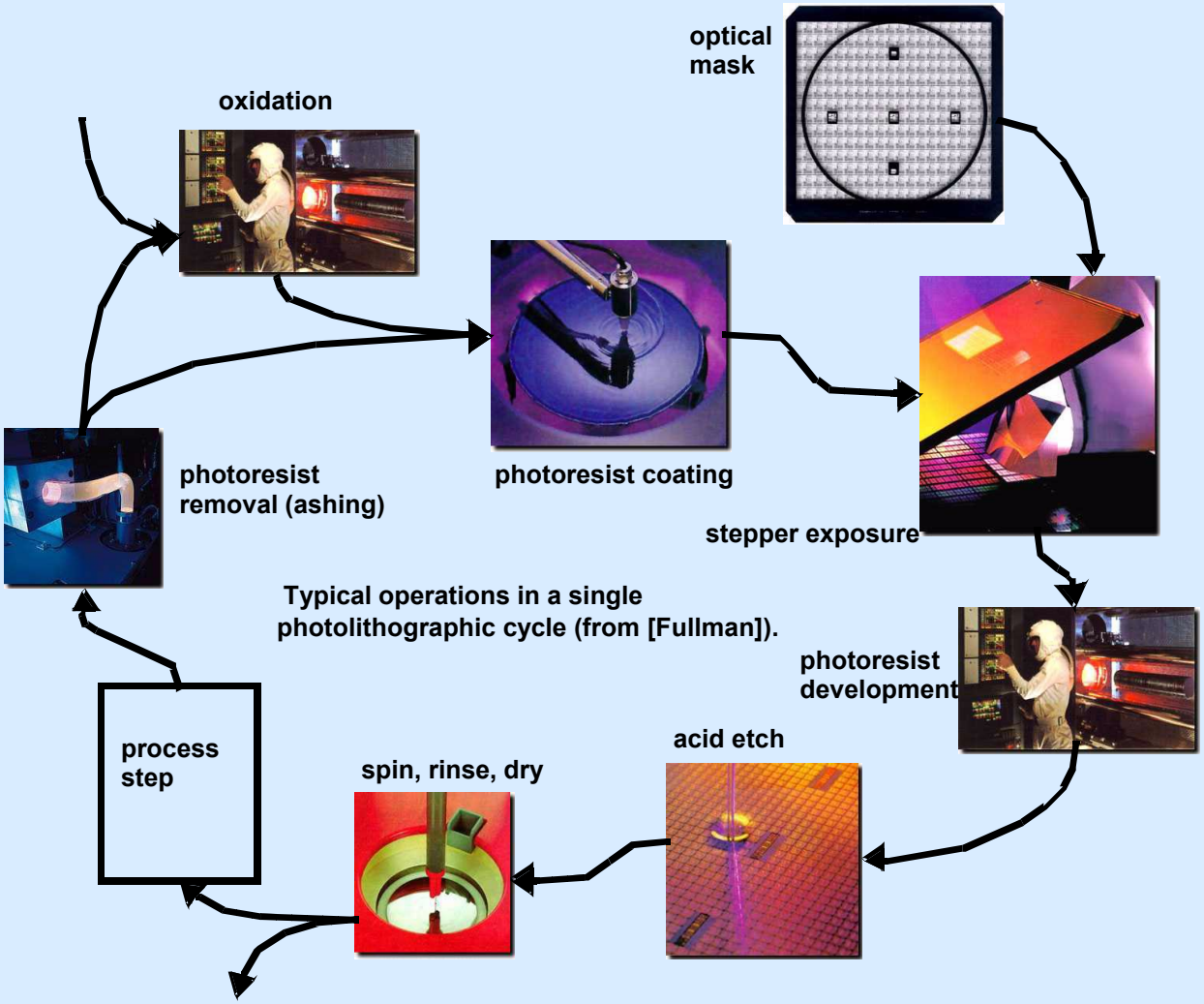
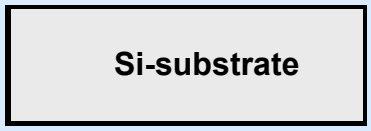


Photo-Lithographic Process

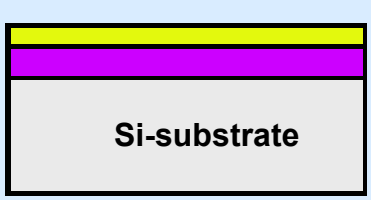


Typical operations in a single photolithographic cycle (from [Fullman]).

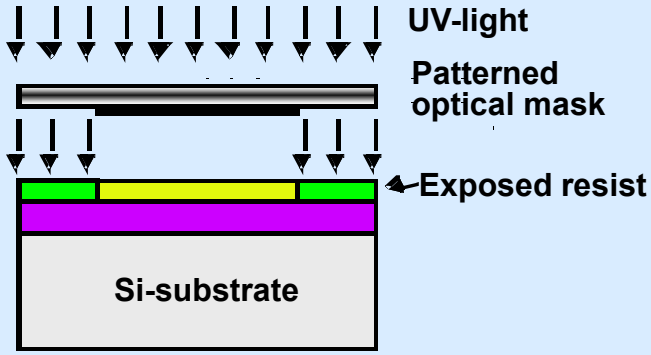
Patterning of SiO_2



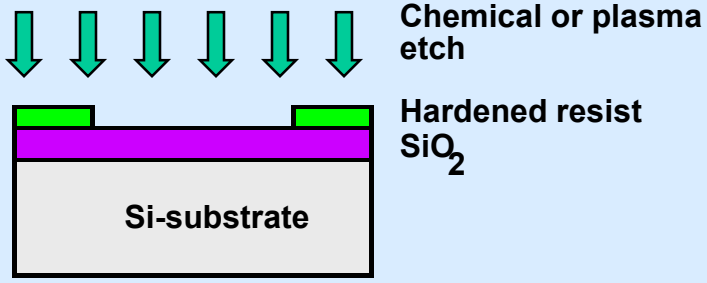
(a) Silicon base material



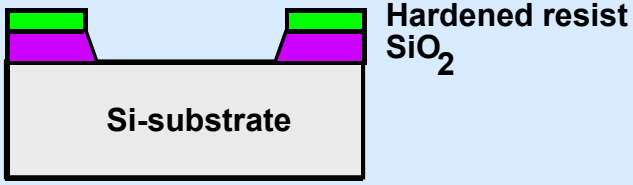
(b) After oxidation and deposition of negative photoresist



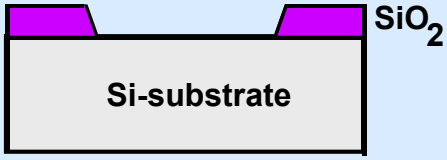
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2

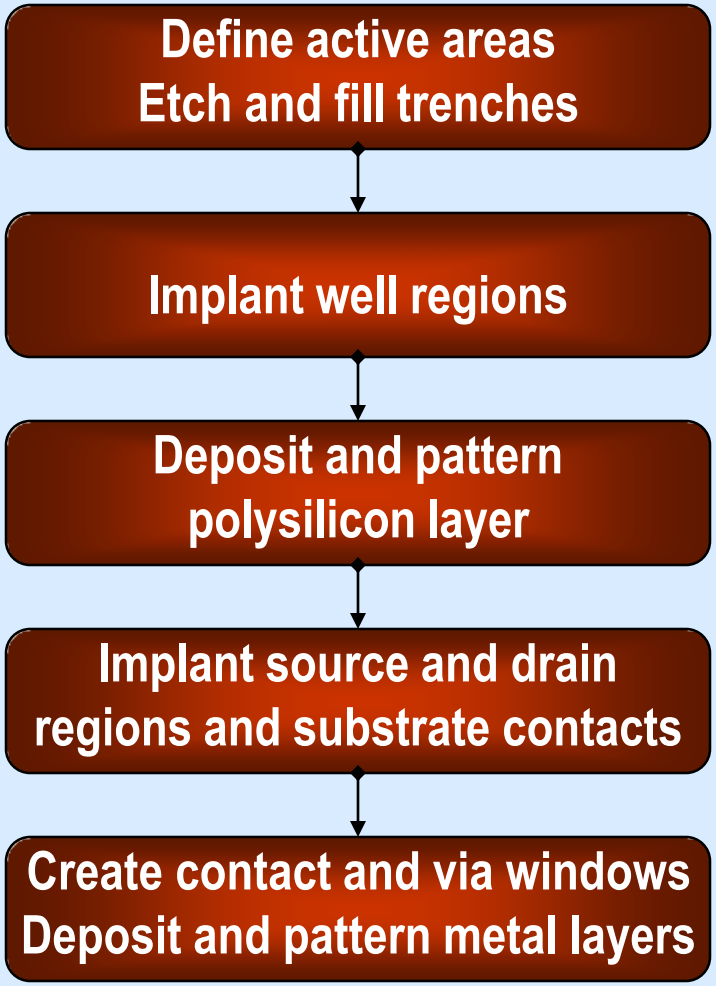


(e) After etching

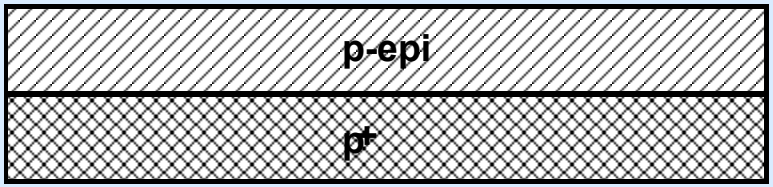


(f) Final result after removal of resist

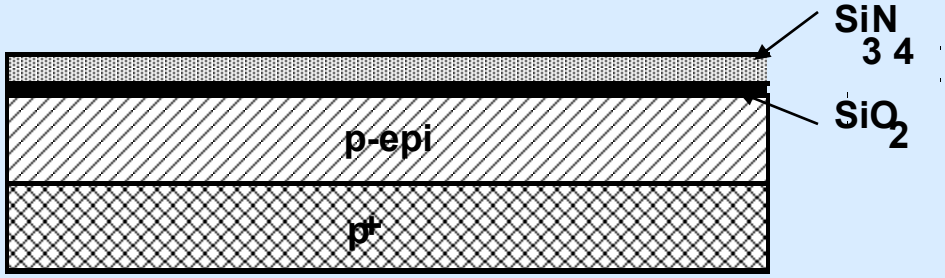
CMOS Process at a Glance



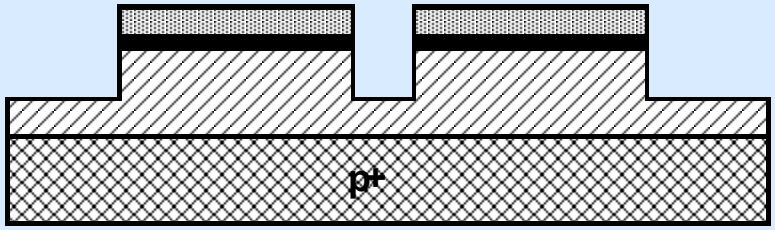
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

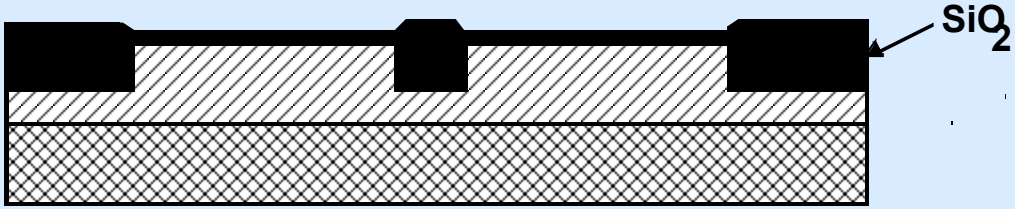


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

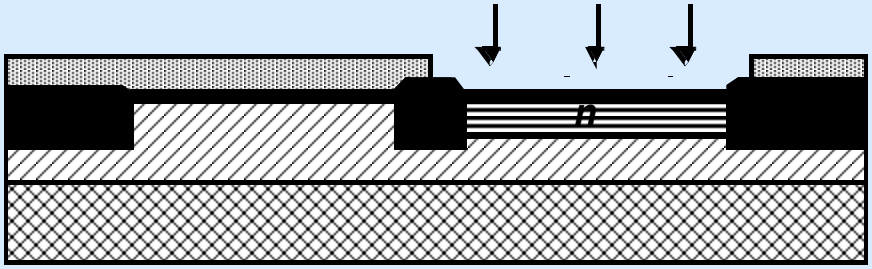


(c) After plasma etch of insulating trenches using the inverse of the active area mask

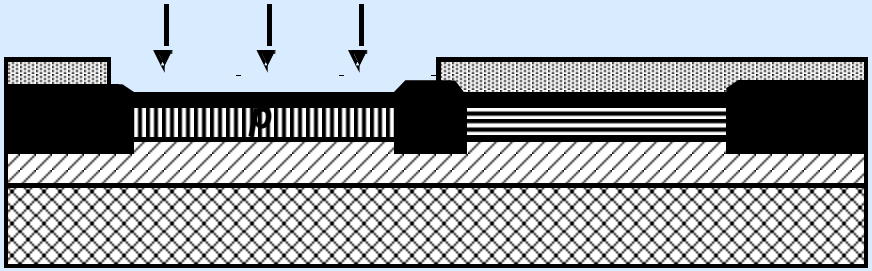
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

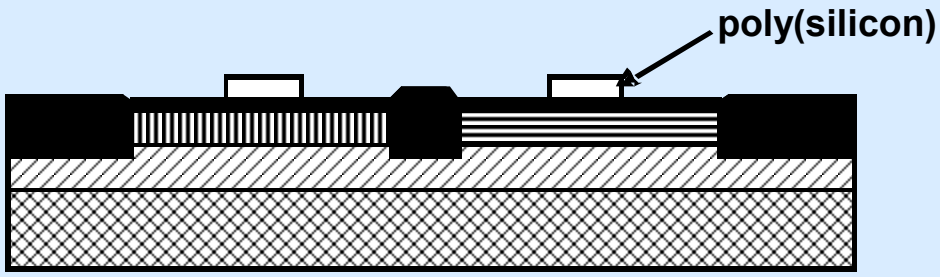


(e) After n-well and V_{TP} adjust implants

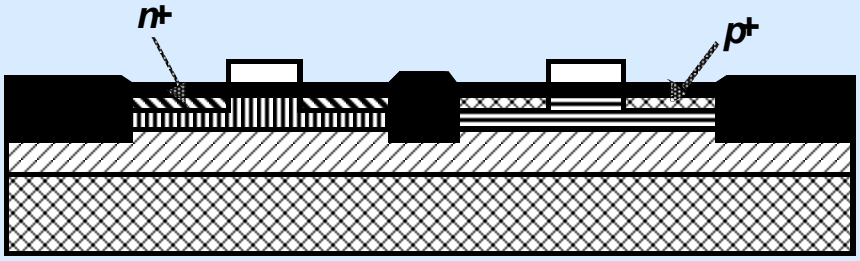


(f) After p-well and V_{TN} adjust implants

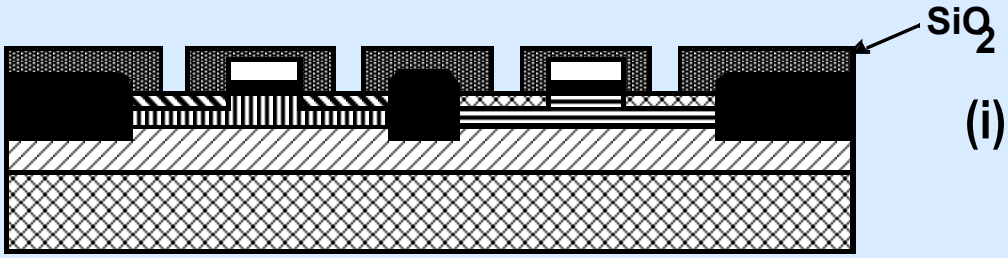
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

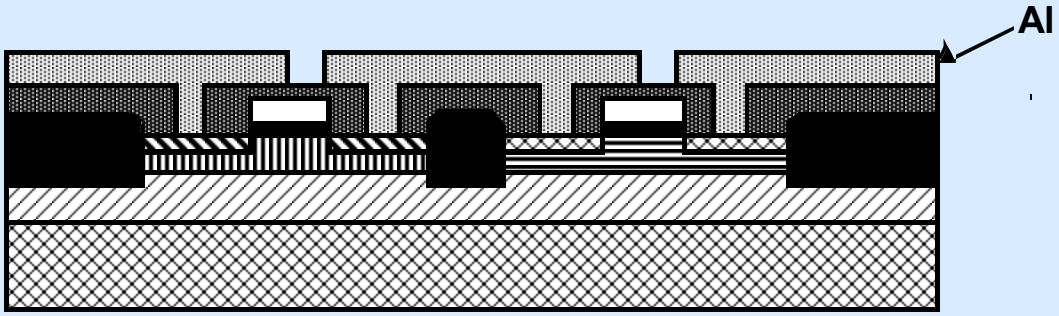


(h) After n+ source/drain and p+ source/drain implants. These steps also dope the polysilicon.

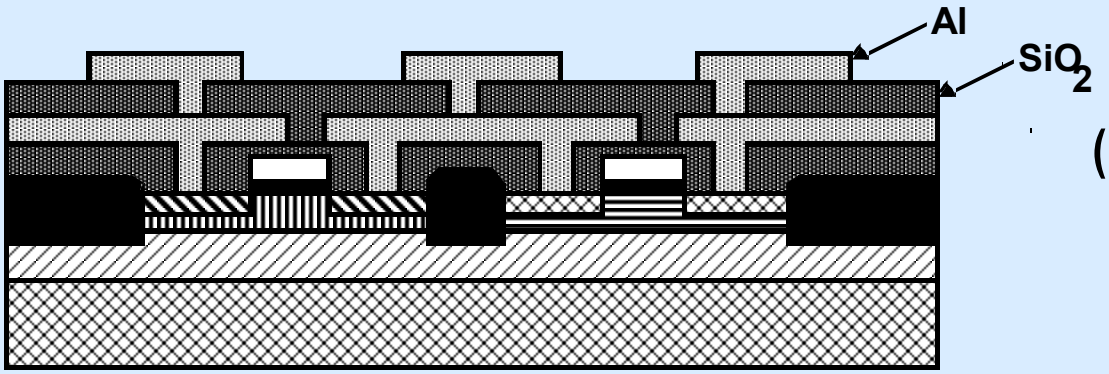


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through



(j) After deposition and patterning of first Al layer.



(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

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