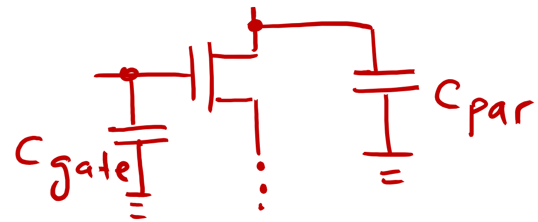
ECE115C – Digital Electronic Circuits

Lecture 4:

CMOS Inverter VTC

Lecture 3 Summary

- **Gate capacitance**
- **Diffusion capacitance**



$$\boxed{\begin{array}{c} C_{par},\ C_{gate} \sim W \\ \hline \gamma = \dfrac{C_{par}}{C_{gate}} \end{array}}$$

$C_{gate} \sim 2\ \text{fF}/\mu\text{m}$
$C_{par} \sim 1.5\ \text{fF}/\mu\text{m}$

tech parameter
~ 0.75

- $R_{on} = \frac{3}{4}\frac{V_{DSAT}}{I_{DSAT}}\left(1 - \frac{7}{9}\lambda V_{DD}\right)$

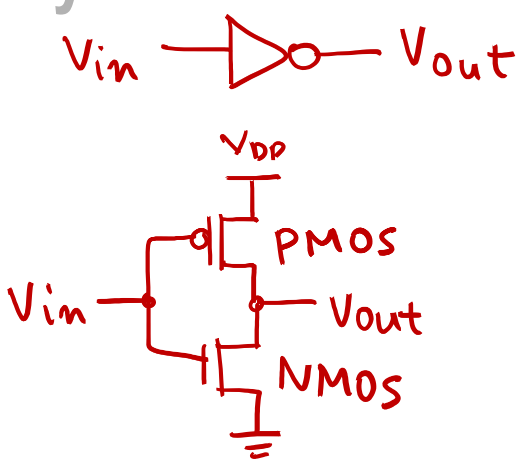
$$\boxed{R_{on} \sim W^{-1}}$$

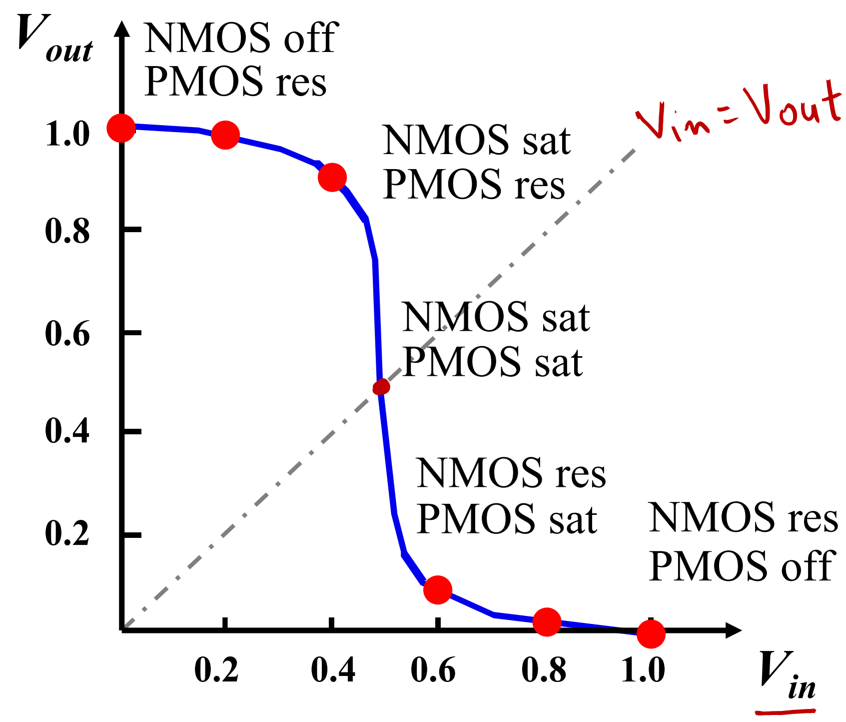
Four Key Design Metrics for Digital ICs

- Cost of ICs
- <u>Reliability</u>
- Speed
- Power

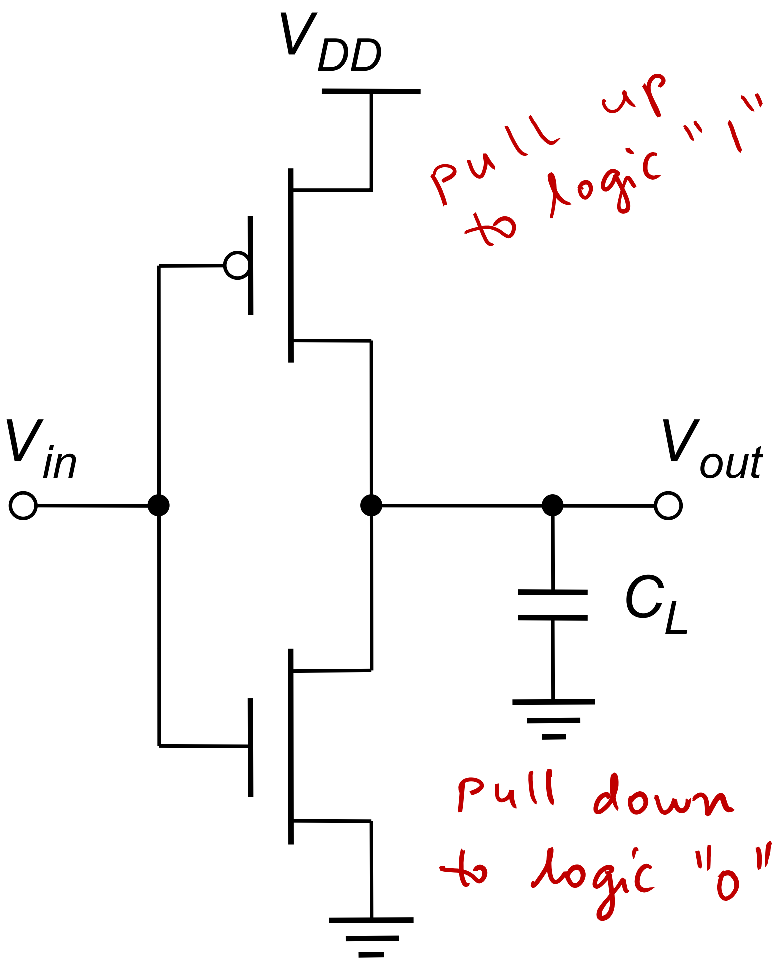
Agenda

- **CMOS Inverter – Static VTC**
- Reliability



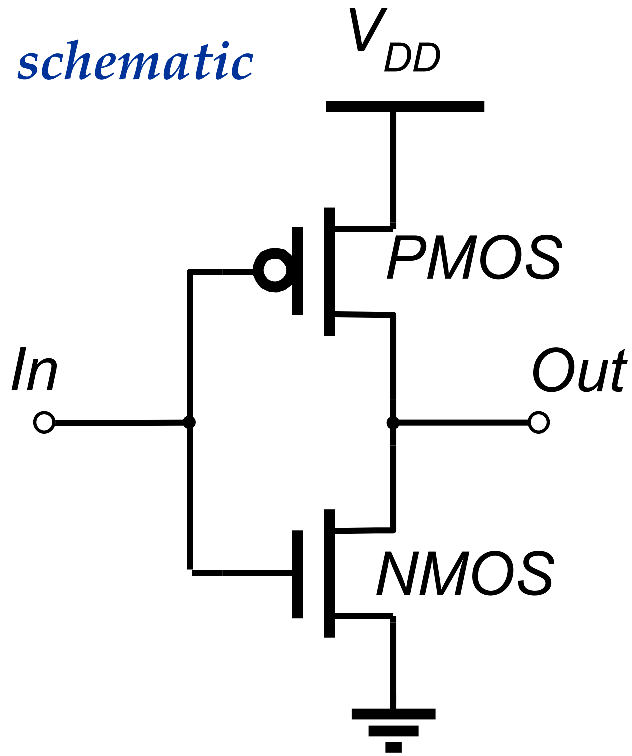


The CMOS Inverter: A First Glance

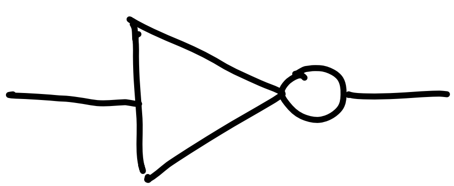


CMOS Inverter

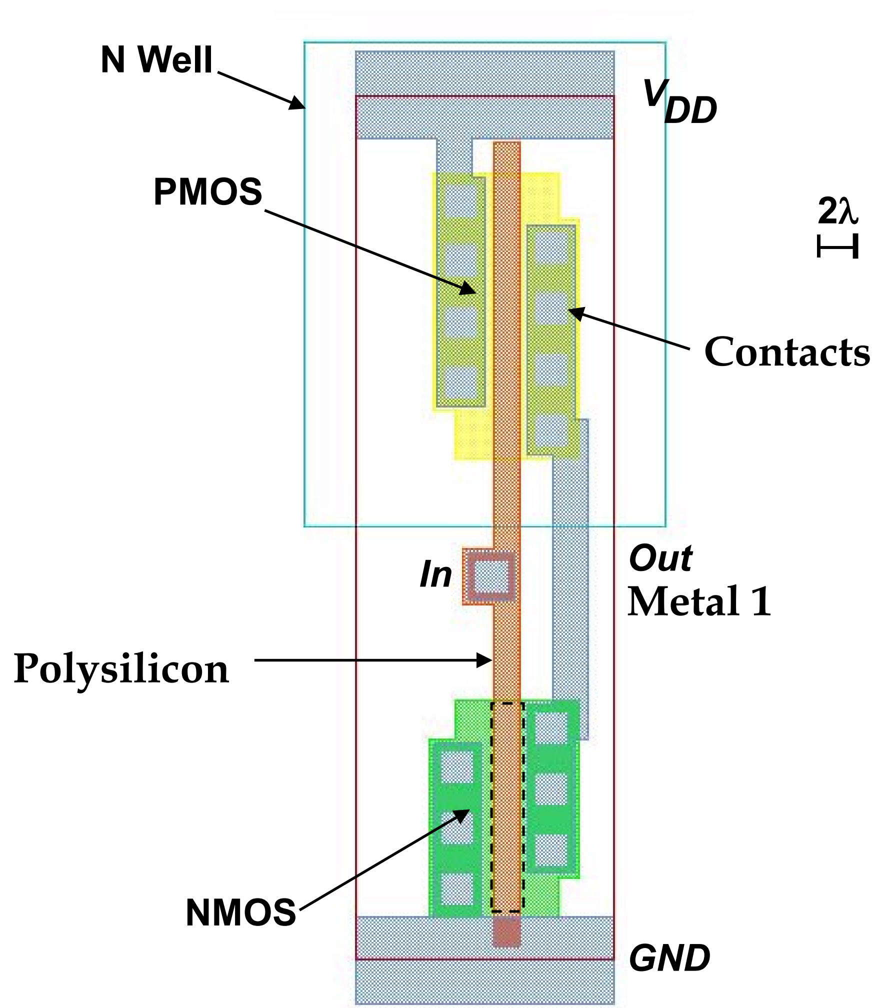
schematic



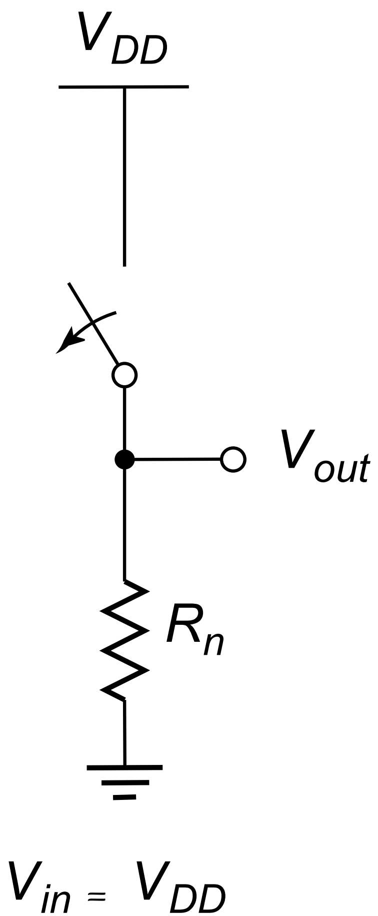
symbol

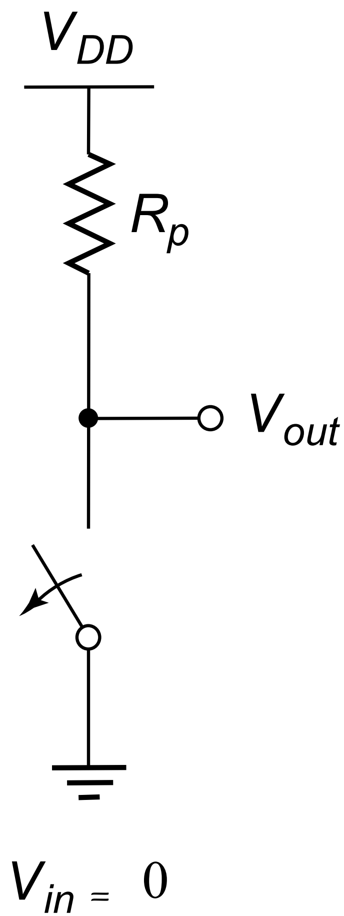


layout



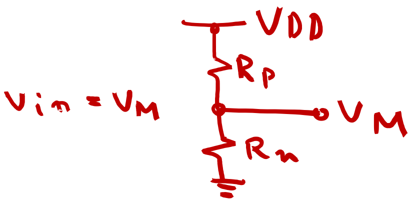
CMOS Inverter: First Order DC Analysis





$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

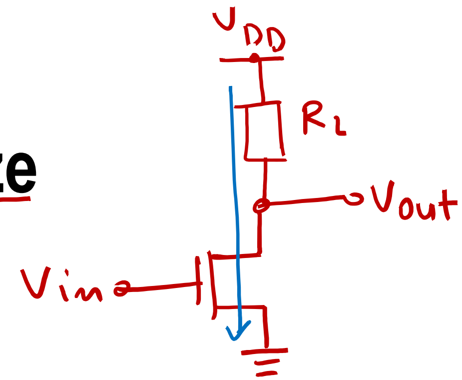
$V_{in} = V_{out} = V_M$



CMOS Properties

- Full rail-to-rail swing
  - $V_{OH} = V_{DD}, V_{OL} = 0$
- Logic levels independent on transistor size
  - "Ratioless" logic
- Low output resistance (kΩ range)
- High input resistance
- No direct-path current in steady state (ignoring leakage)

$\tau \sim \underbrace{R}_{k\Omega \; 10^{3}} \; \underbrace{C}_{fF \; 10^{-15}} \; (\sim ps \; 10^{-12})$



$V_{OH} = V_{DD}$
(NMOS off)

$\Rightarrow V_{OL} = \frac{R_n}{R_n + R_L} V_{DD}$
(NMOS on)

$V_{OL} \neq 0V$

Agenda

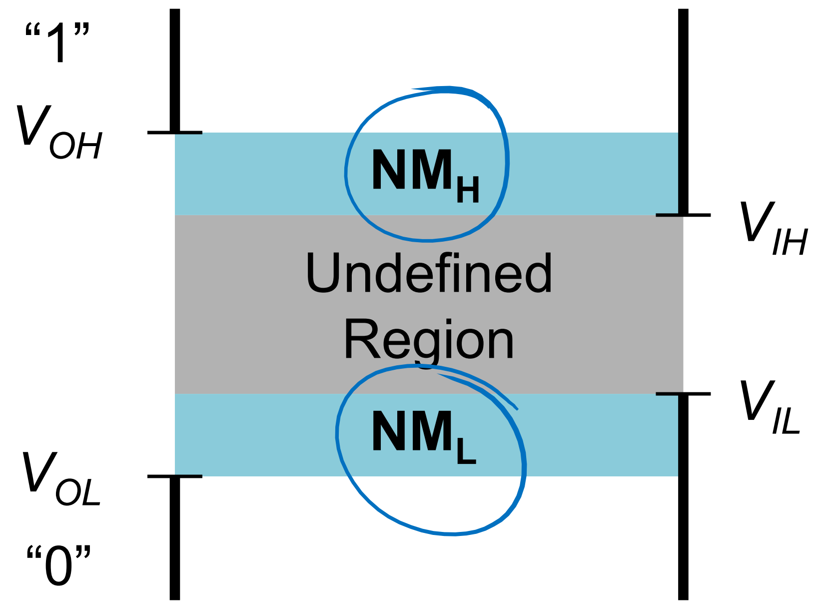
- CMOS Inverter – Static VTC
- **Reliability**

  * Voltge levels

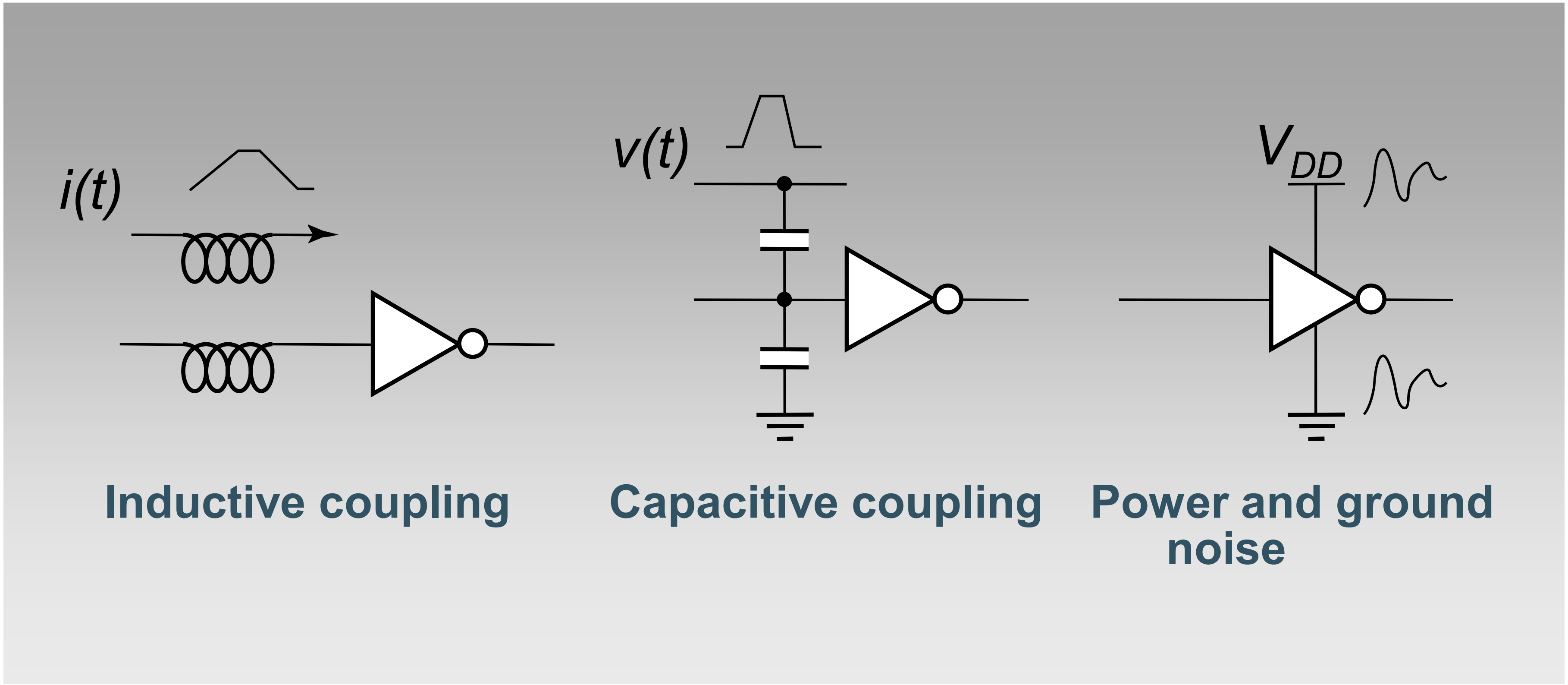
  → Out : V_{OH}, V_{OL}

  → In : V_{IH}, V_{IL}

  * Noise margins

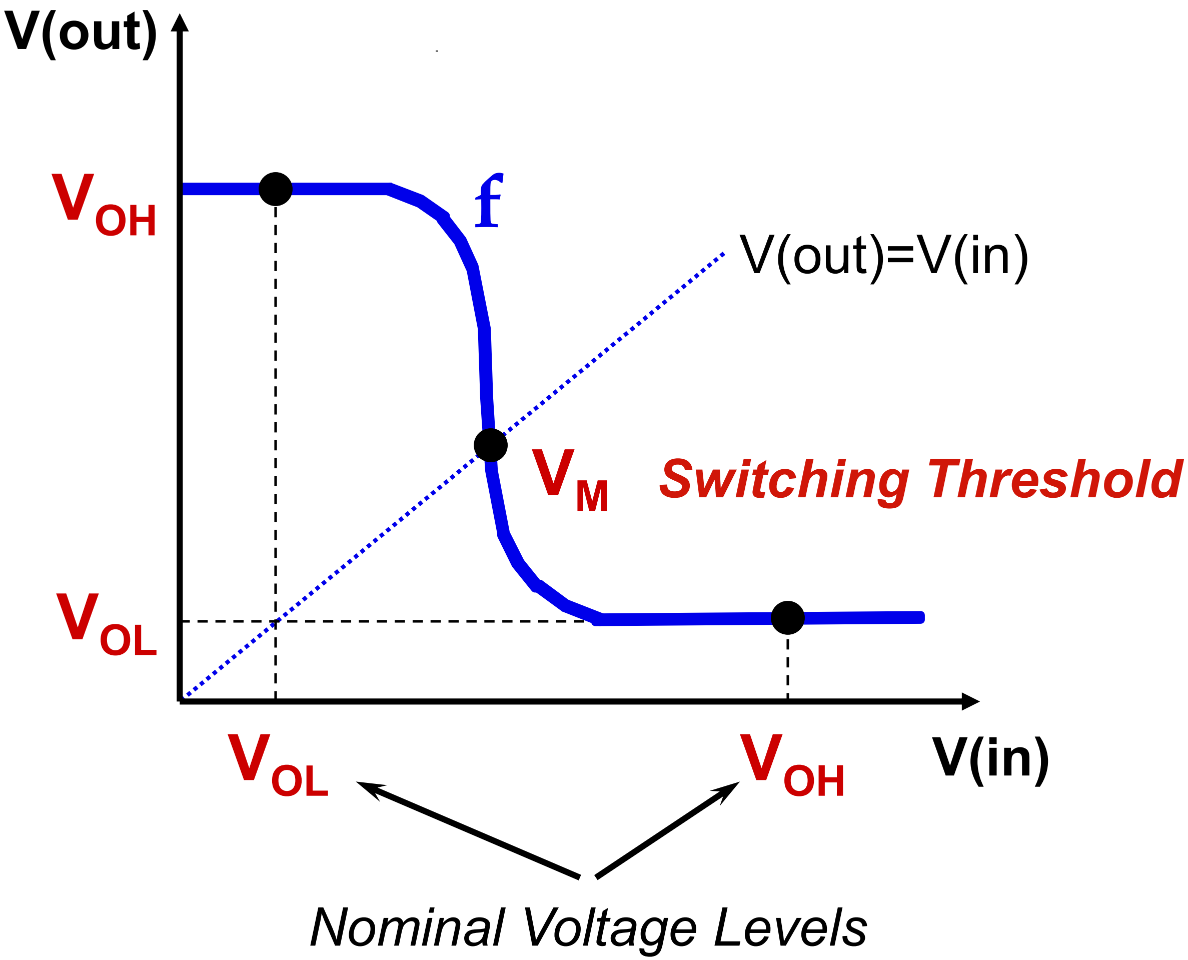


Reliability – Noise in Digital ICs



- **Noise sources**
  - Internal (~ signal swing)
  - External (not related to signal levels)

DC Operation:
Voltage Transfer Characteristic

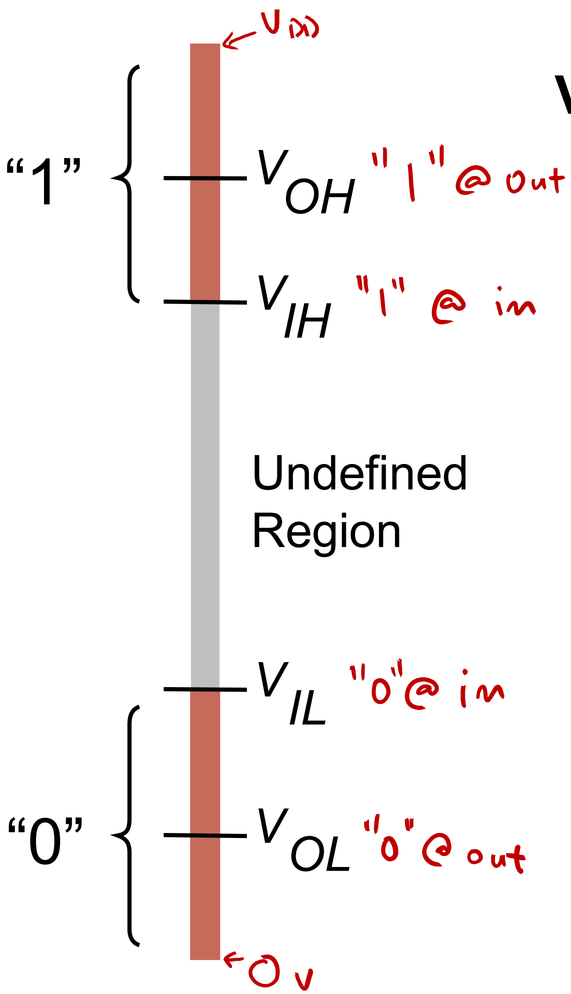


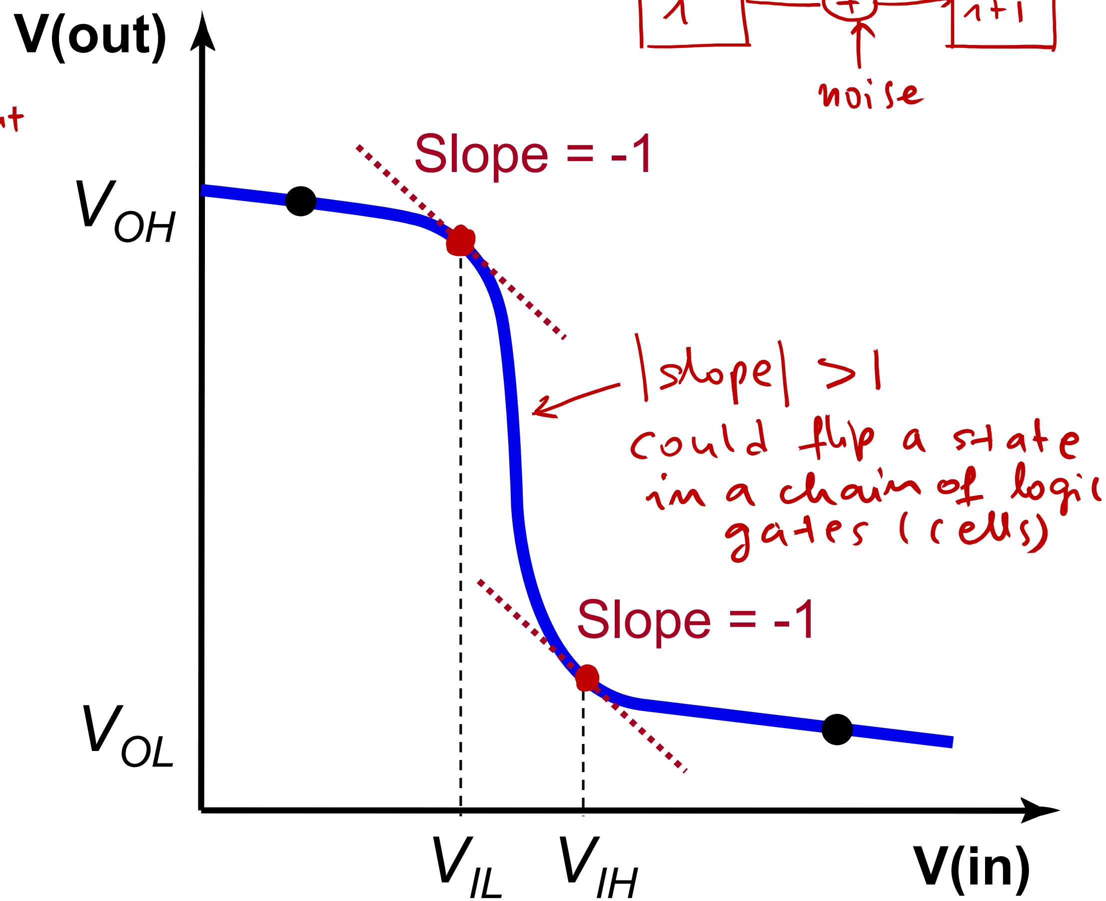
$V_{OH} = f(V_{OL})$

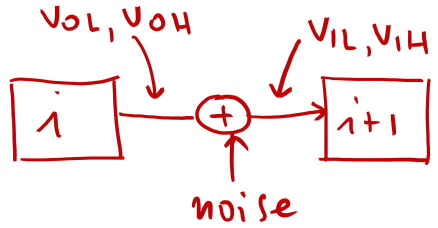
$V_{OL} = f(V_{OH})$

$V_M = f(V_M)$

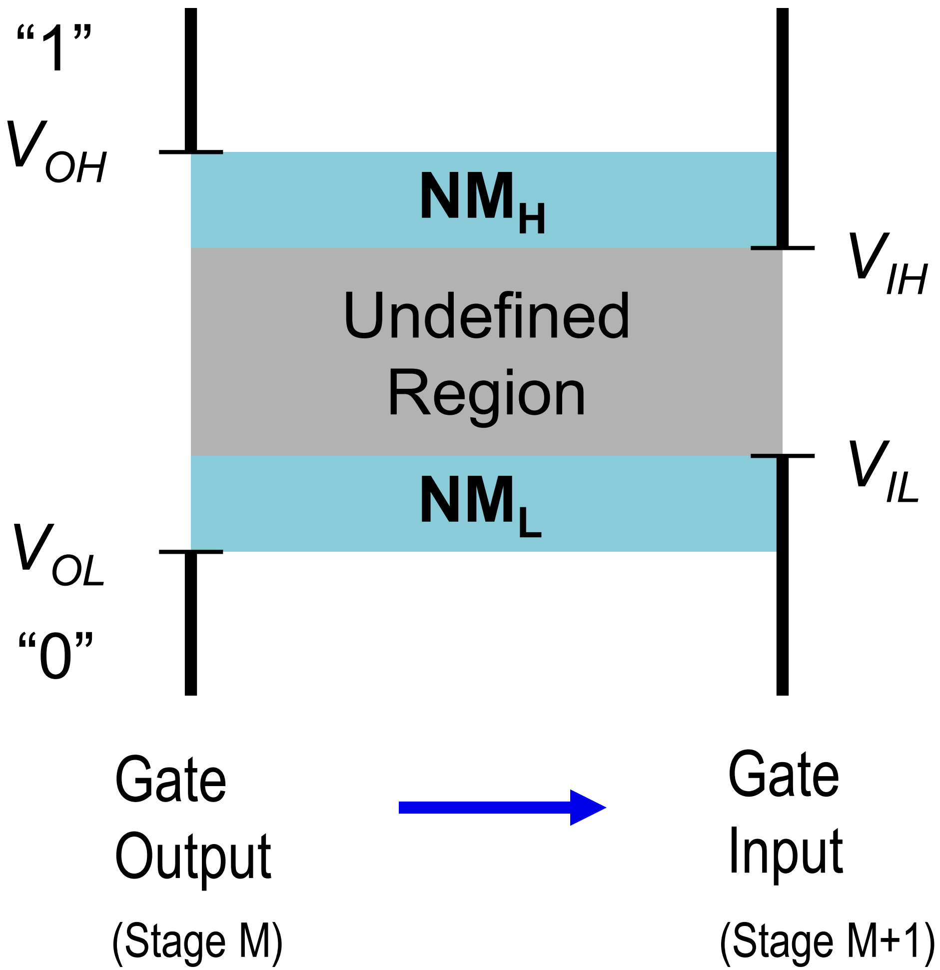
Mapping Between Analog and Digital Signals







Definition of Noise Margins



Noise margin high:

$$NM_H = V_{OH} - V_{IH}$$

Noise margin low:

$$NM_L = V_{IL} - V_{OL}$$

Noise Budget

- Allocates gross noise margin to expected sources of noise
- Sources
  - power supply
  - offset
  - cross talk
  - interference
  - timing
- Differentiate between fixed and proportional noise sources

Key Reliability Properties

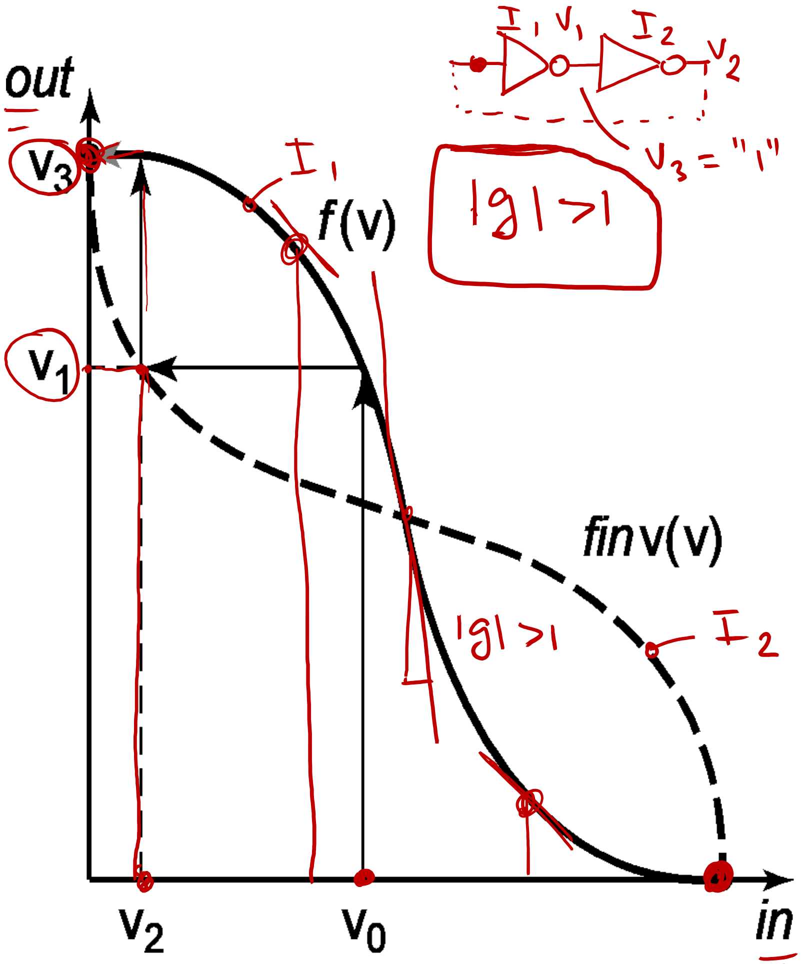
- **Absolute noise margin values are deceptive**
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)

- **Noise immunity is the more important metric – the capability to suppress noise sources**

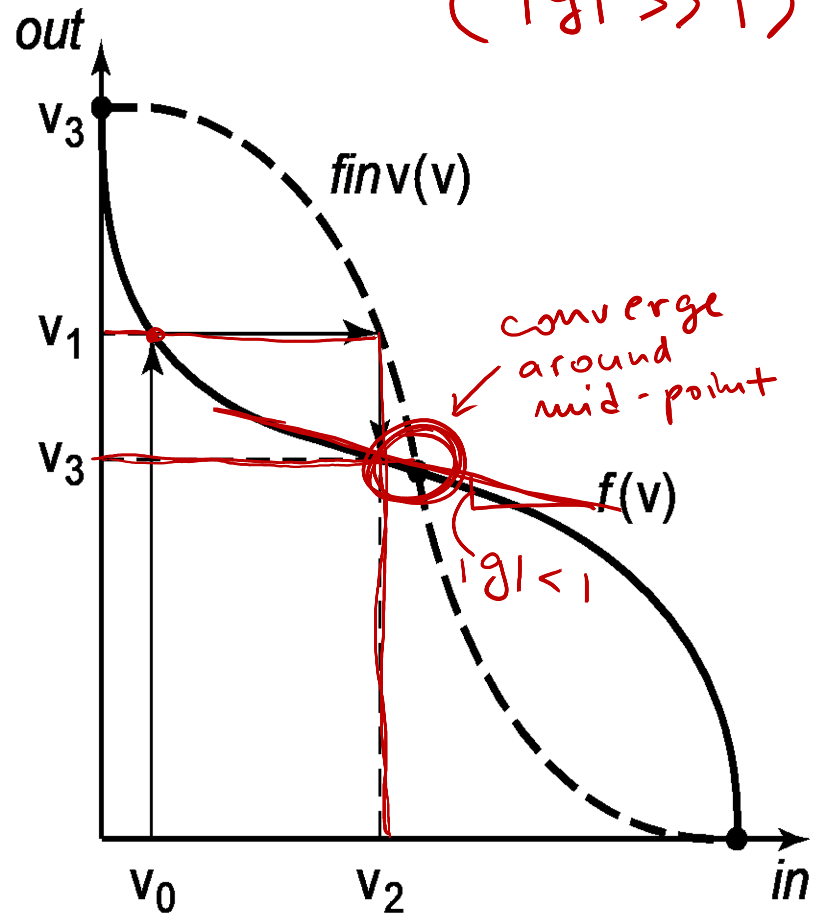
- **Key metrics:**
  - Noise transfer functions
  - Output impedance of the driver
  - Input impedance of the receiver

Regenerative Property ⇒ MUST HAVE |g|>1

(|g| >> 1)



Regenerative

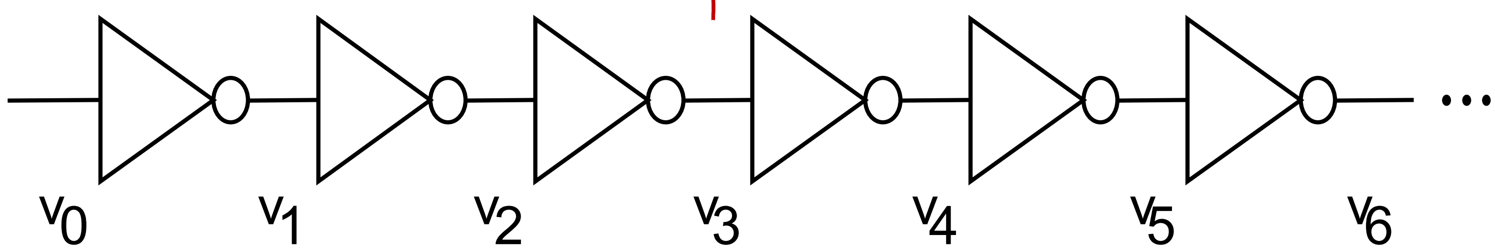


Non-Regenerative

Regenerative Property

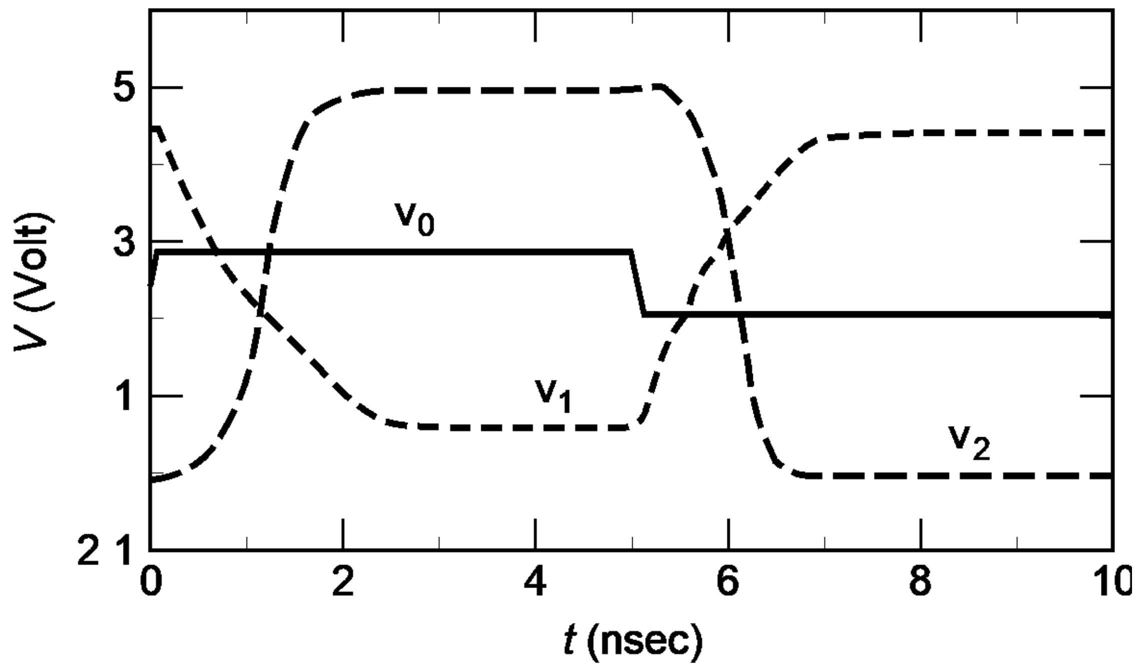
A chain of inverters

full swing



signal regeneration
level

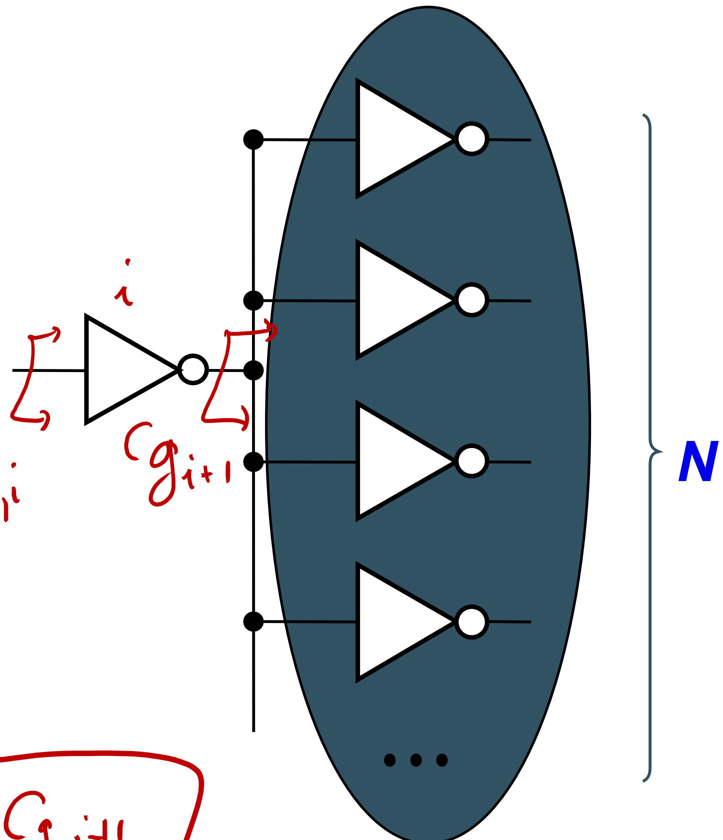
Simulated response



Fan-In and Fan-Out

$i+1$

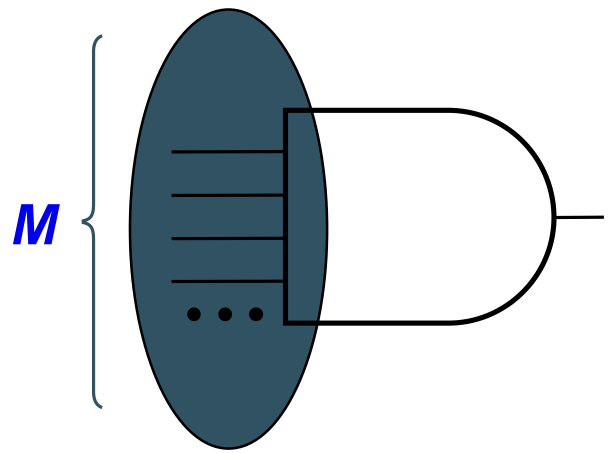
i



$C_{g,i}$ $C_{g,i+1}$

$\boxed{\dfrac{C_{g,i+1}}{C_{g,i}}}$

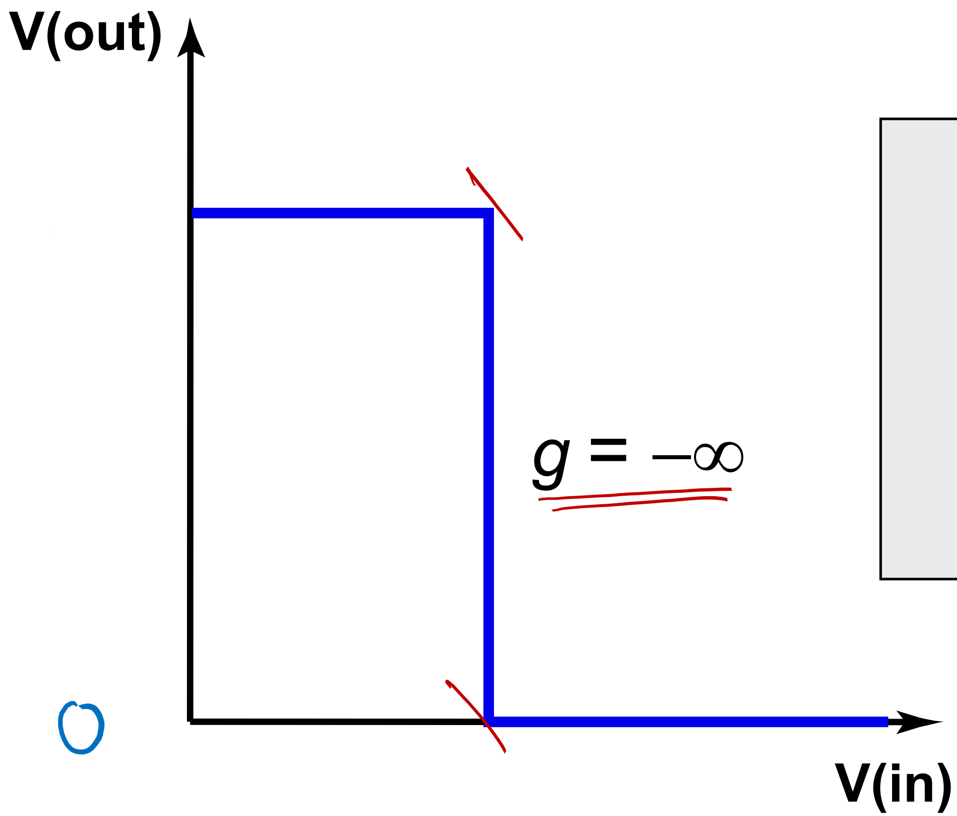
Fan-out *N*



Number of logic inputs

Fan-in *M*

The Ideal Gate



$R_i = \infty$

$R_o = 0$

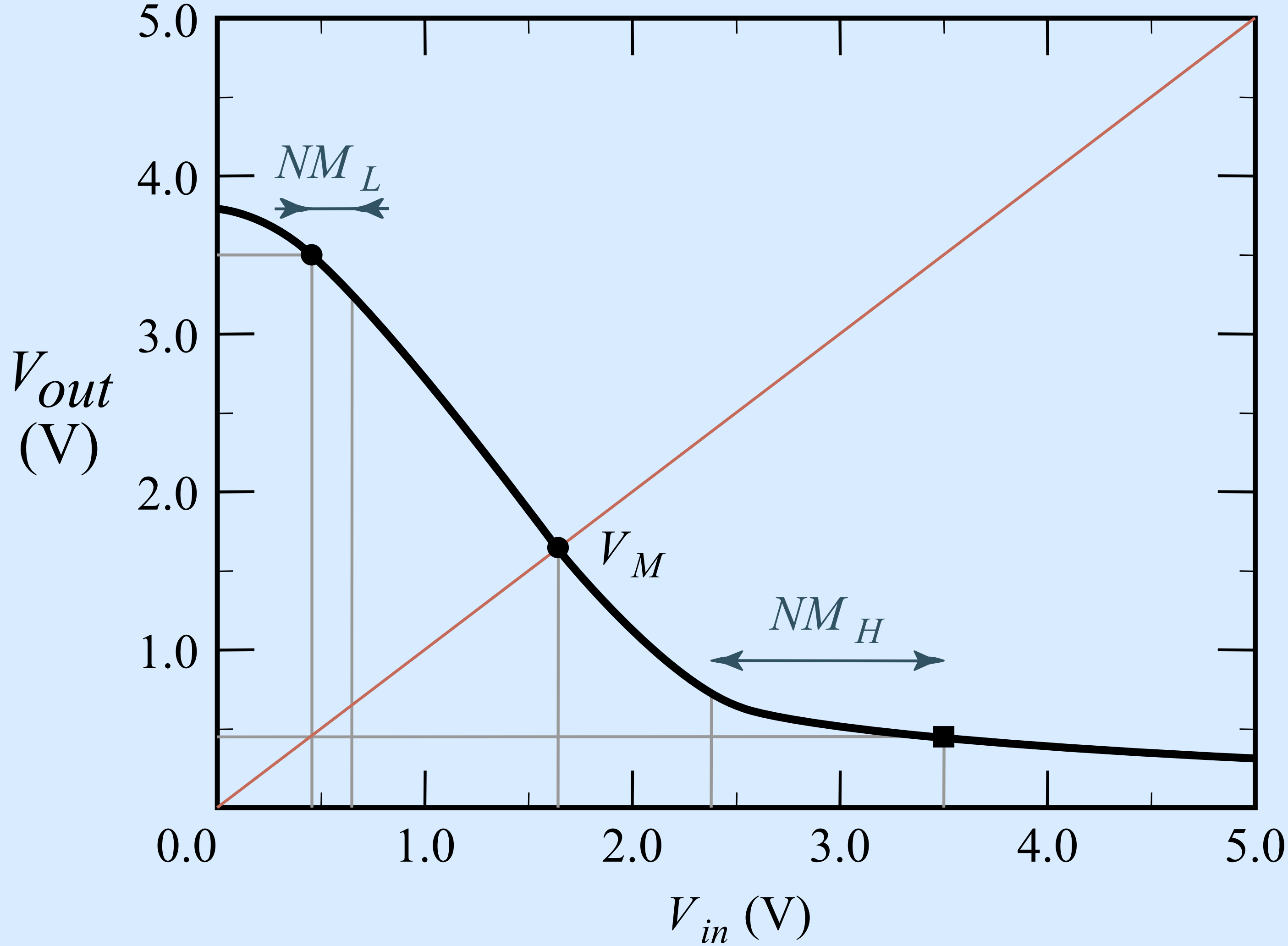
Fanout $= \infty$

$NM_H = NM_L = V_{DD}/2$

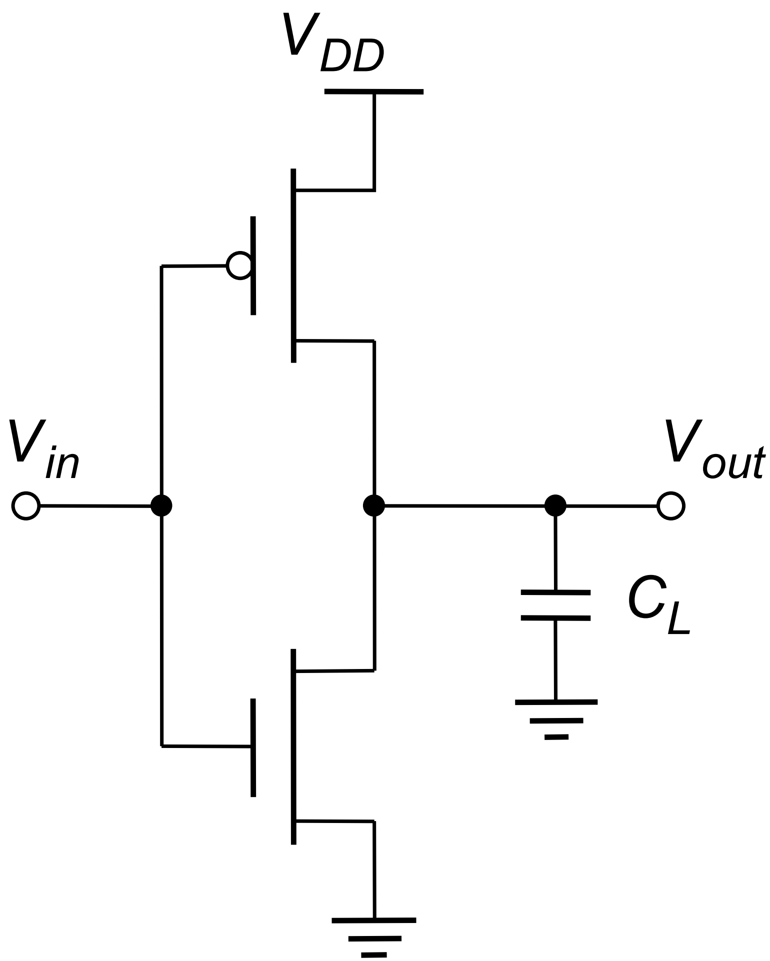
$V_{OL} = 0$, $V_{OH} = V_{DD}$

$V_{IL} = V_{IH} = \frac{V_{DD}}{2}$

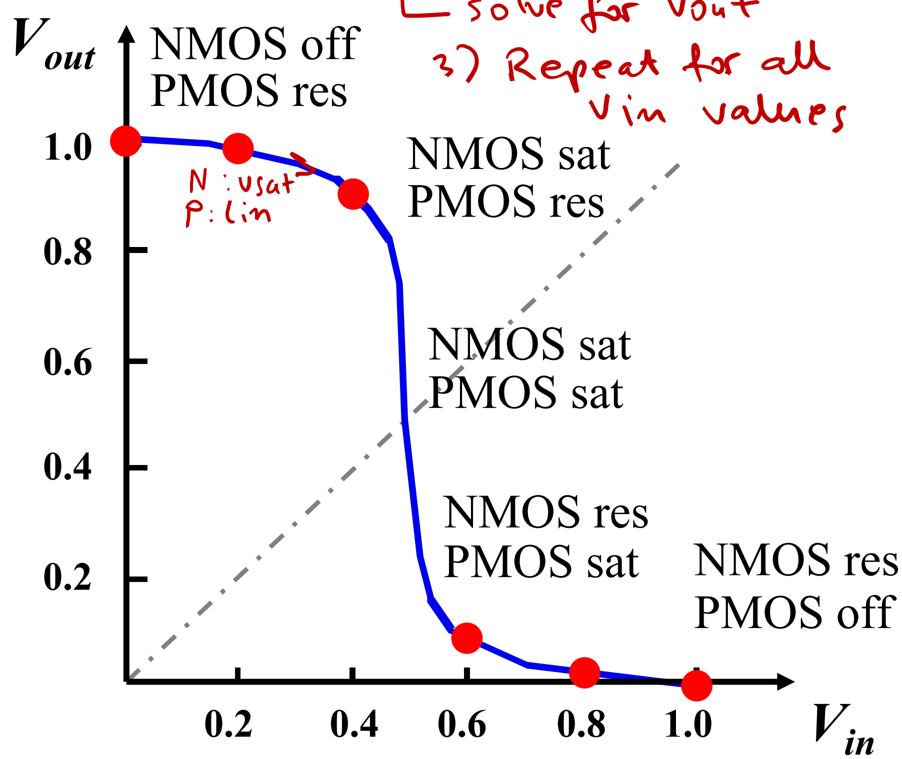
An Old-Time Inverter



CMOS Inverter VTC



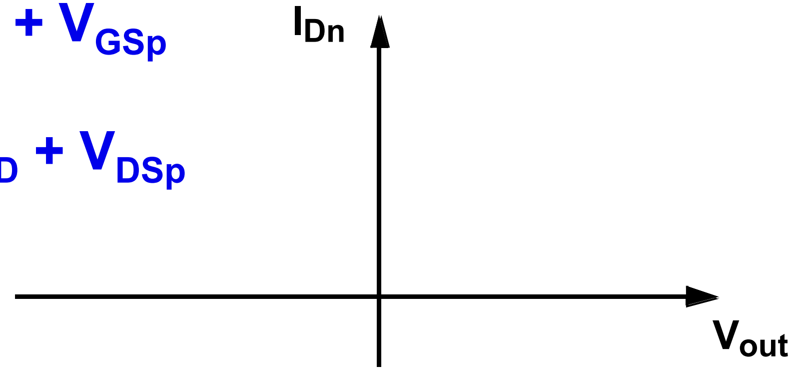
1) Assume Vin, sweep 0 → V_{DD}
2) Op. mode (N, P)
   └ $I_N = I_P$
      └ solve for Vout
3) Repeat for all Vin values

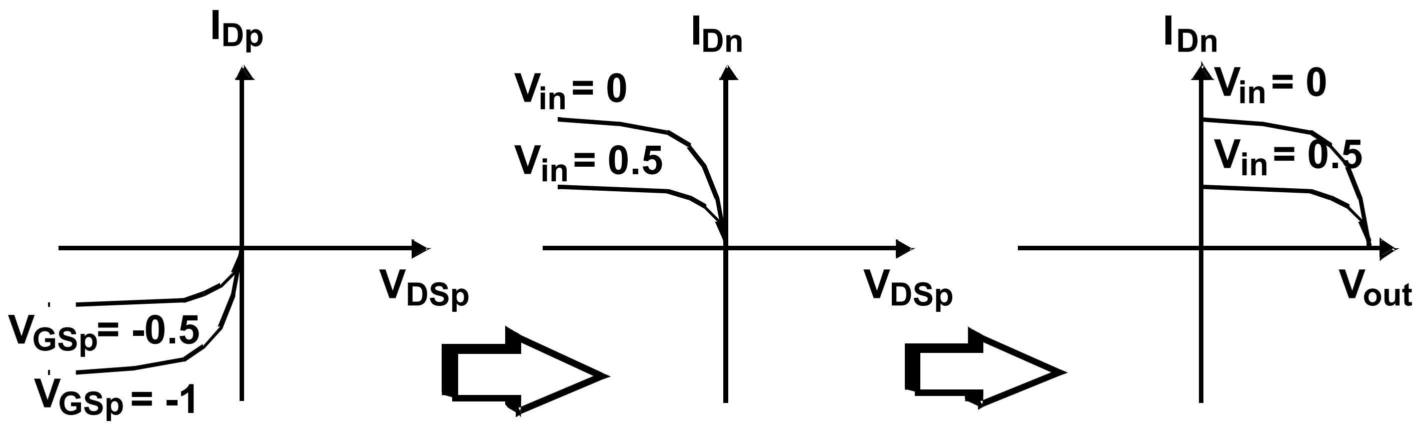


PMOS Load Lines

- **Coordinate transform: $I_{Dp}\ (V_{DSp}) \rightarrow I_{Dn}\ (V_{out})$**

$V_{in} = V_{DD} + V_{GSp}$
$I_{Dn} = -I_{Dp}$
$V_{out} = V_{DD} + V_{DSp}$

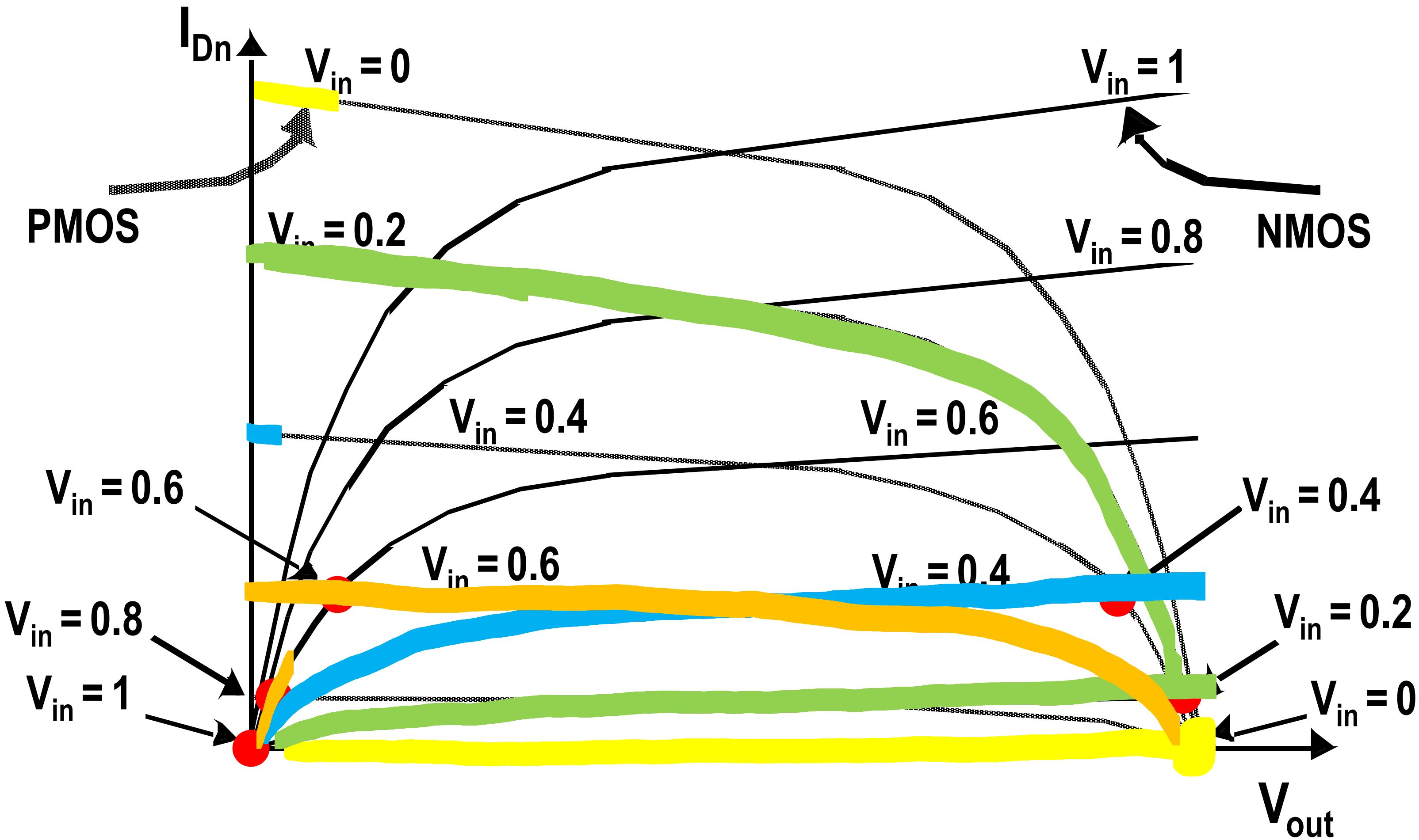




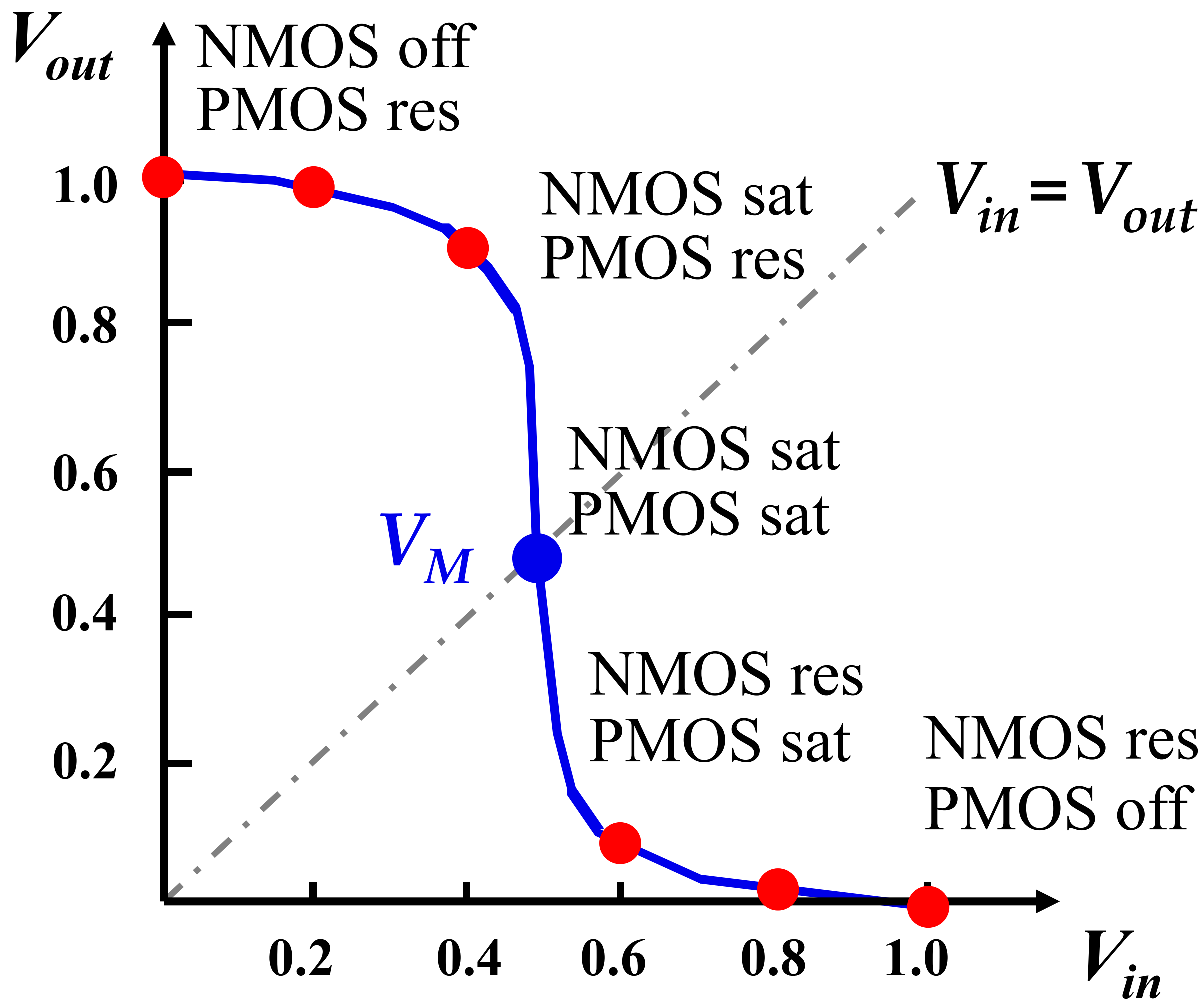
$V_{in} = V_{DD} + V_{GSp}$
$I_{Dn} = -I_{Dp}$

$V_{out} = V_{DD} + V_{DSp}$

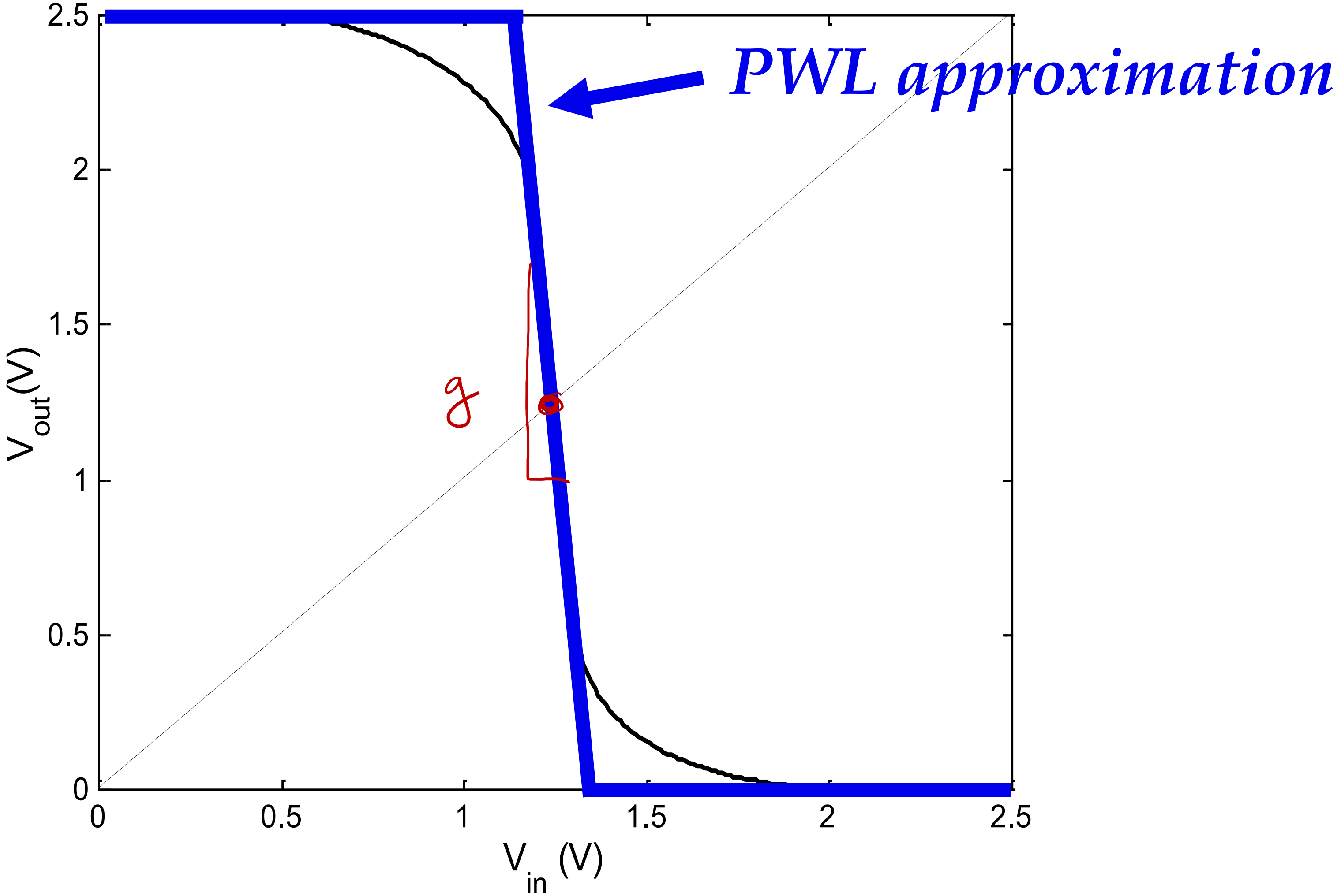
CMOS Inverter Load Characteristics



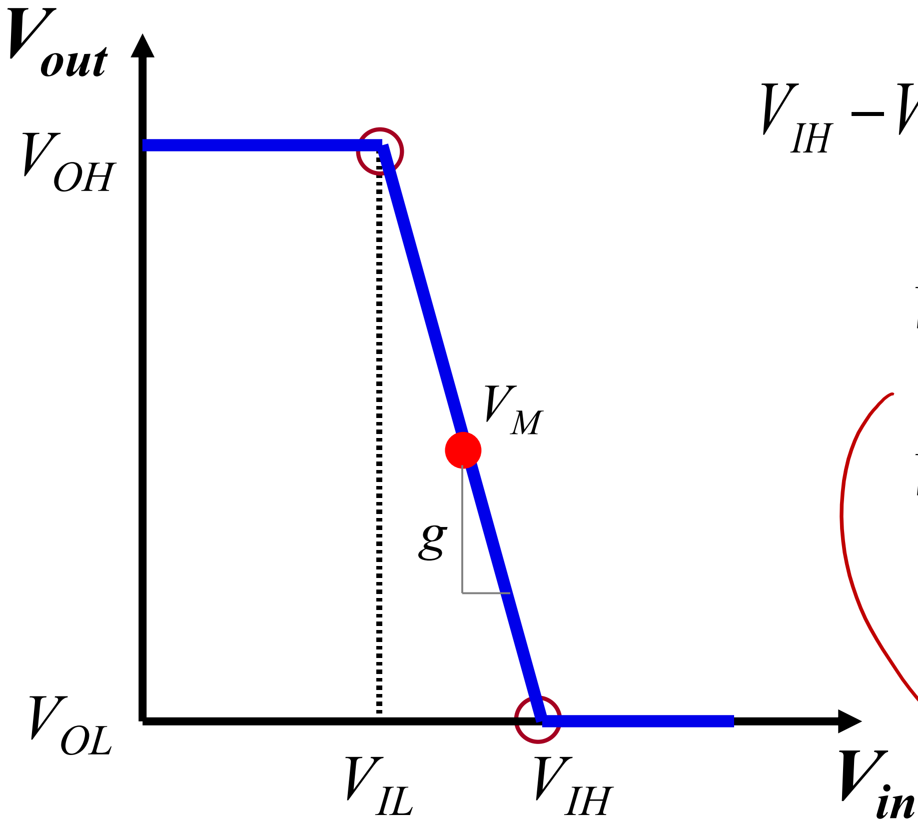
CMOS Inverter VTC



Simulated VTC (PWL Approximation)



Determining V_{IH} and V_{IL}



A simplified approach

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = -\frac{V_{DD}}{g} = \frac{V_{DD}}{|g|}$$

$$V_{IH} = V_M - \frac{V_M - V_{OL}}{g}$$

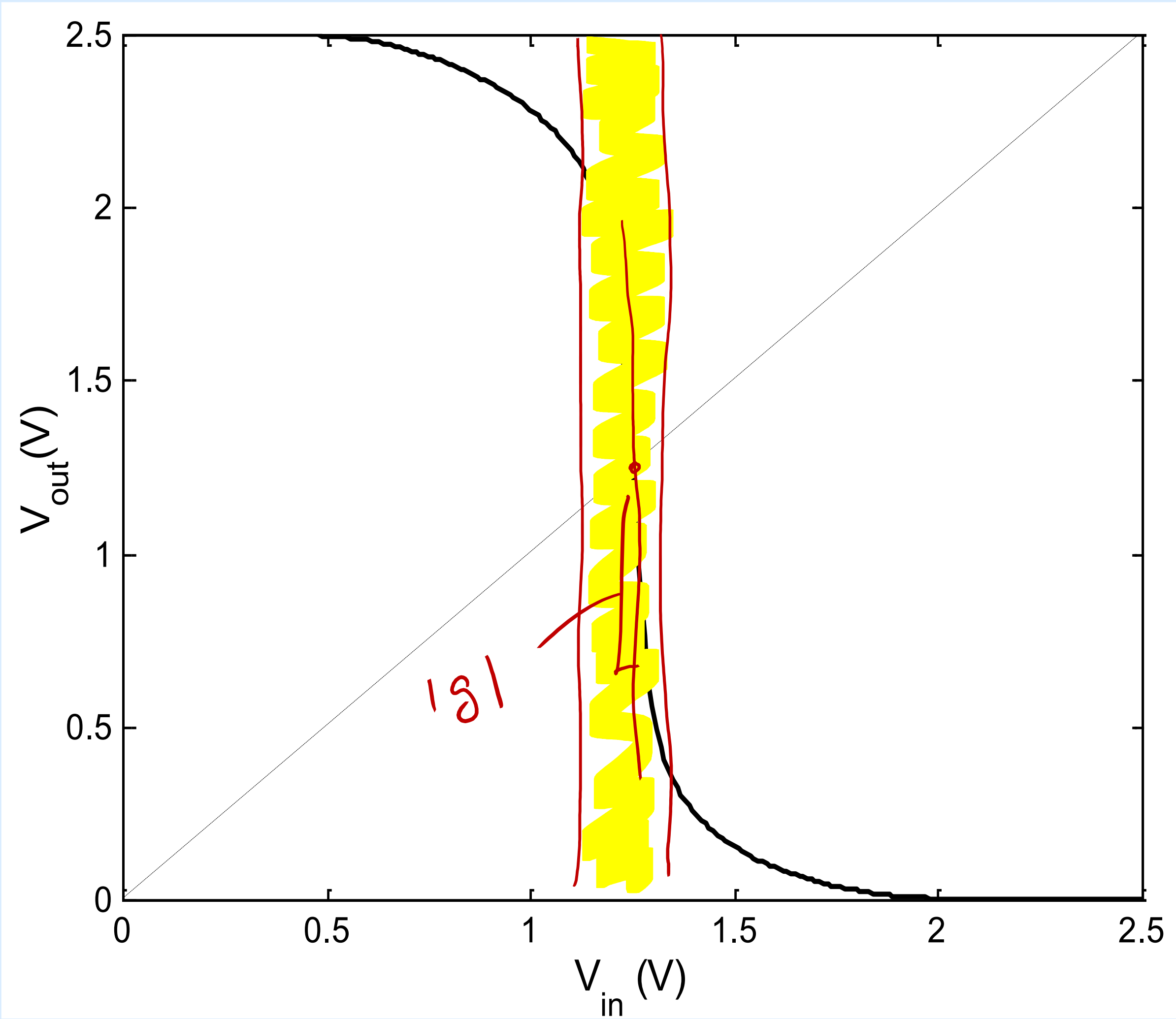
$$V_{IL} = V_M + \frac{V_{OH} - V_M}{g}$$

For $V_{OH} = V_{DD}$, $V_{OL} = 0$:

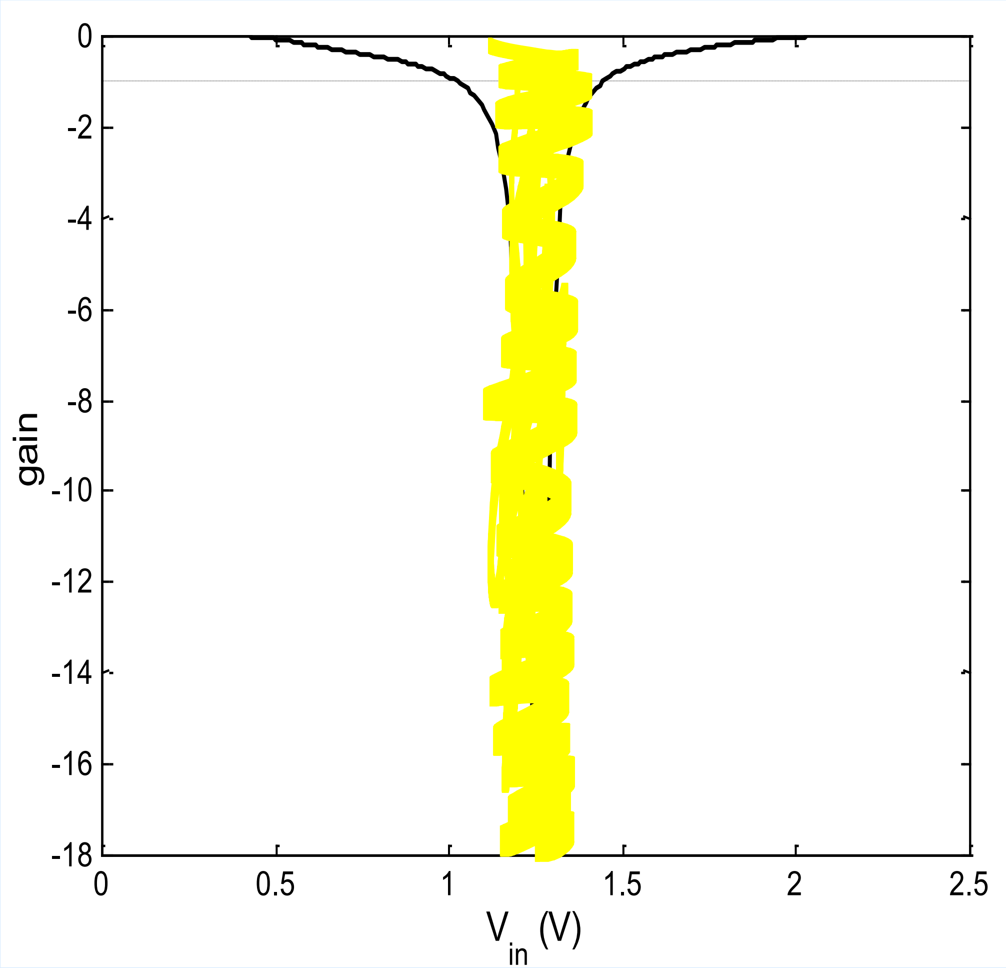
$$NM_H = V_{DD} - V_{IH}$$

$$NM_L = V_{IL}$$

Simulated VTC



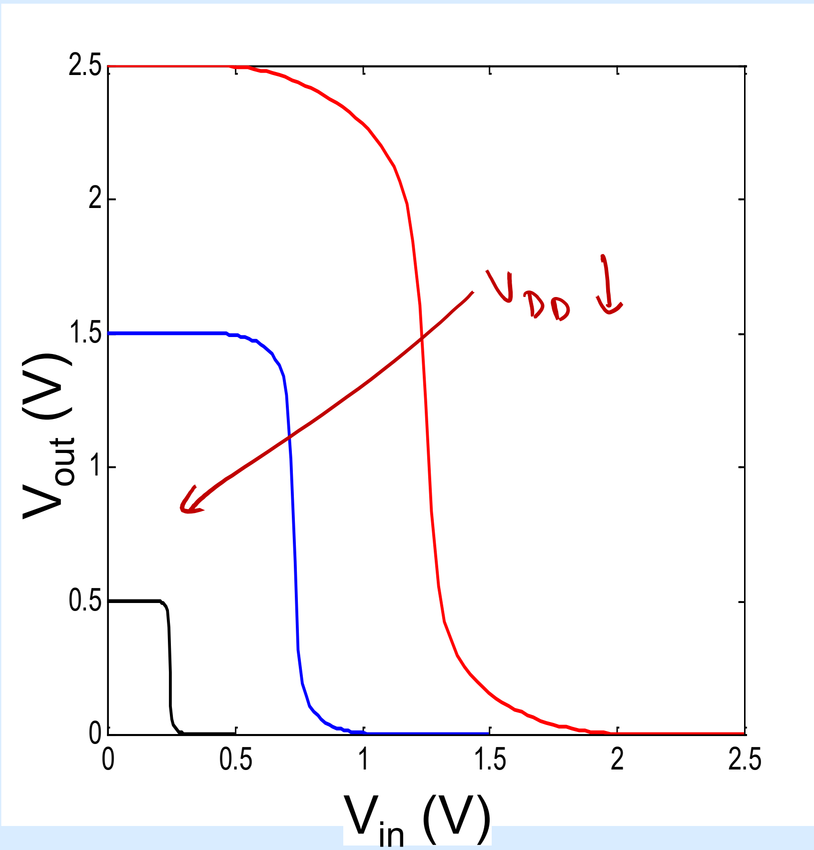
Inverter Gain

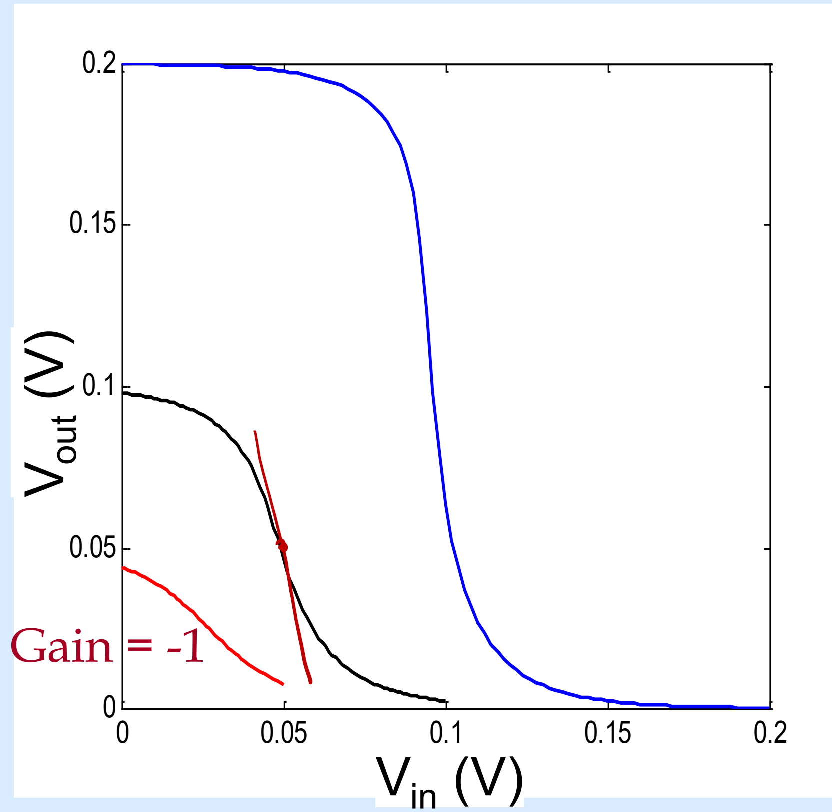


$$g = -\frac{1}{I_D(V_M)} \cdot \frac{k_n \cdot V_{DSATn} + k_p \cdot V_{DSATp}}{\lambda_n - \lambda_p}$$

$$g \approx \frac{1 + r}{(V_M - V_{Tn} - V_{DSATn}/2) \cdot (\lambda_n - \lambda_p)}$$

Gain as a function of V_{DD}

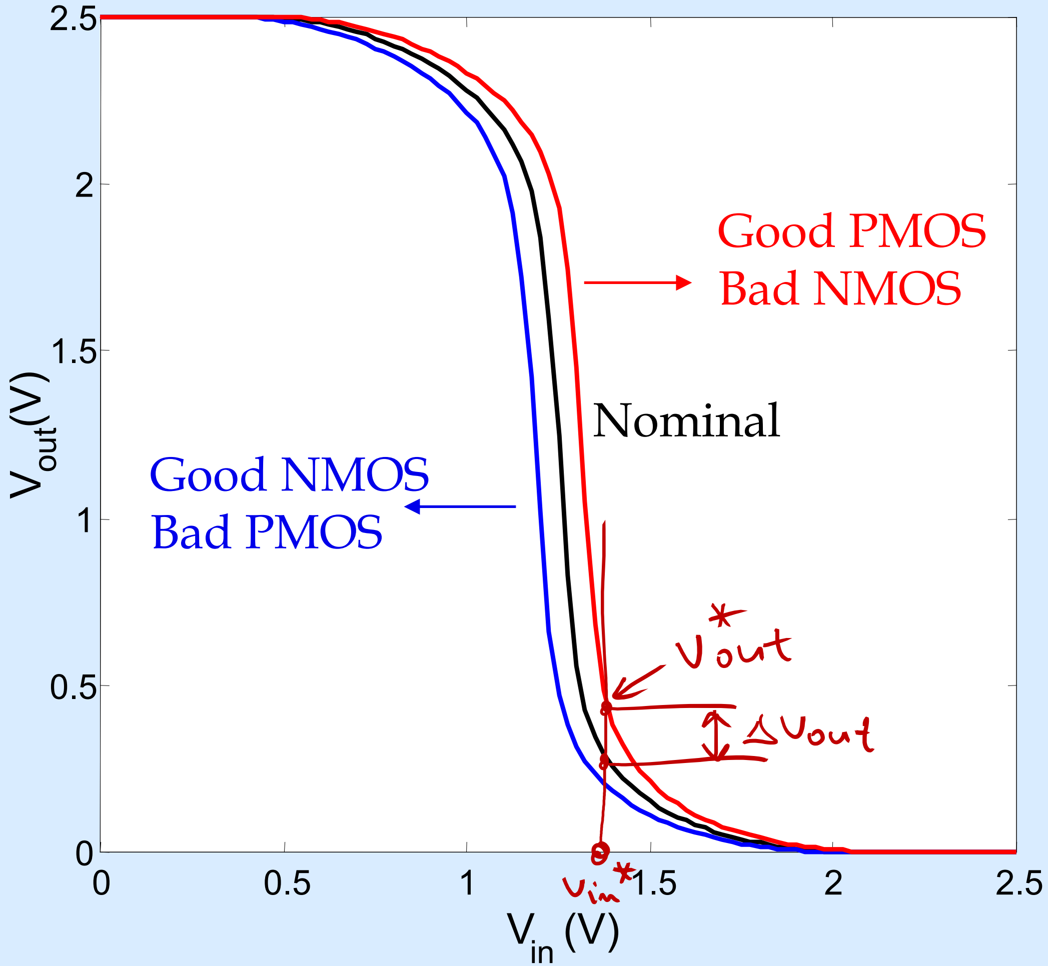


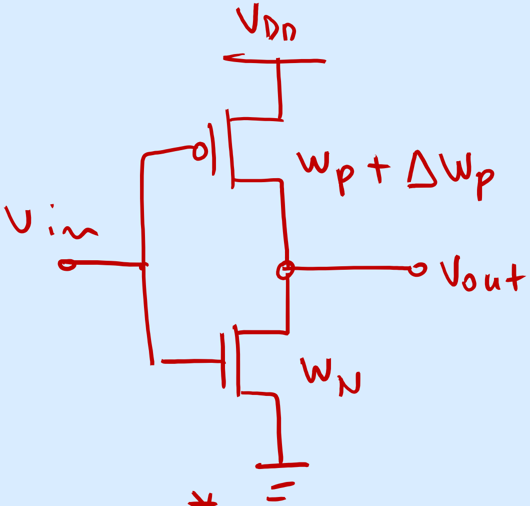


practical $V_{DD,min} \approx 100$ mV

$(4kT/q)$

Impact of Process Variations





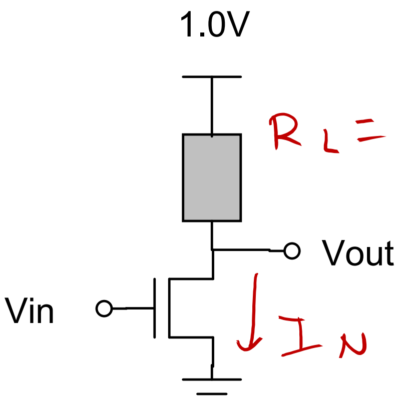
Same V_{in}^*

→ stronger PMOS (ΔW_p)
(more current)

V_{out}^* ↑

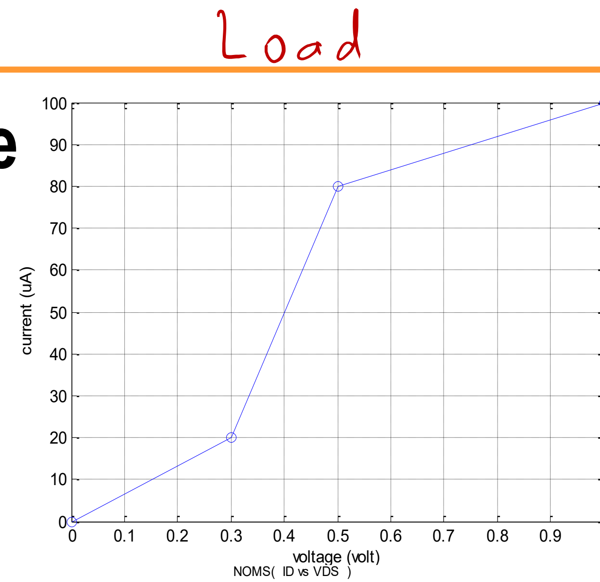
VTC Example

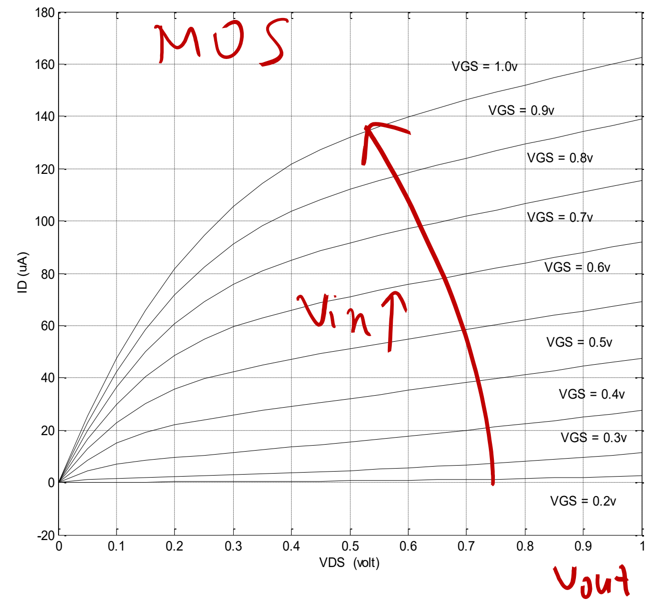
- **NMOS with a non-linear load device**



$R_L = \frac{V_L}{I_L}$

$I_N = I_L$

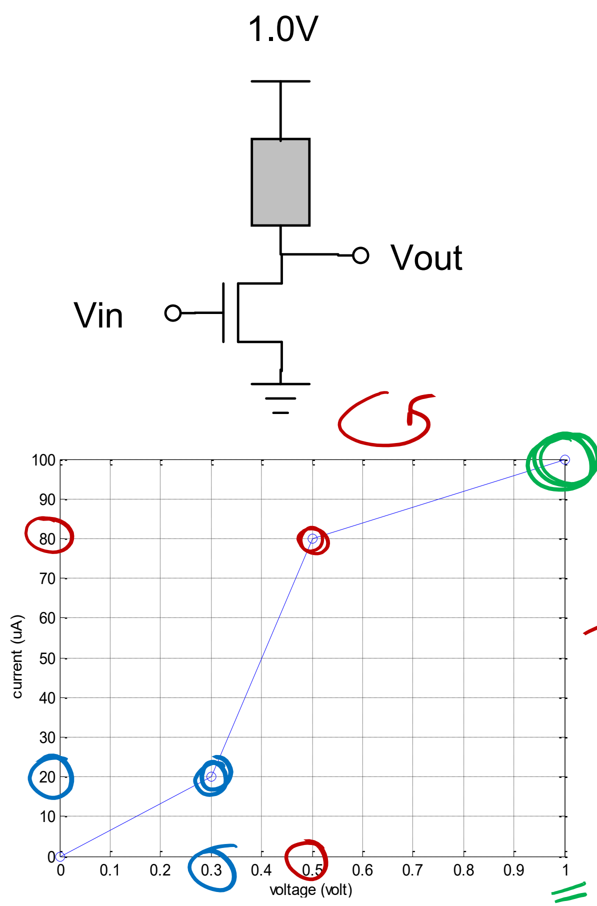


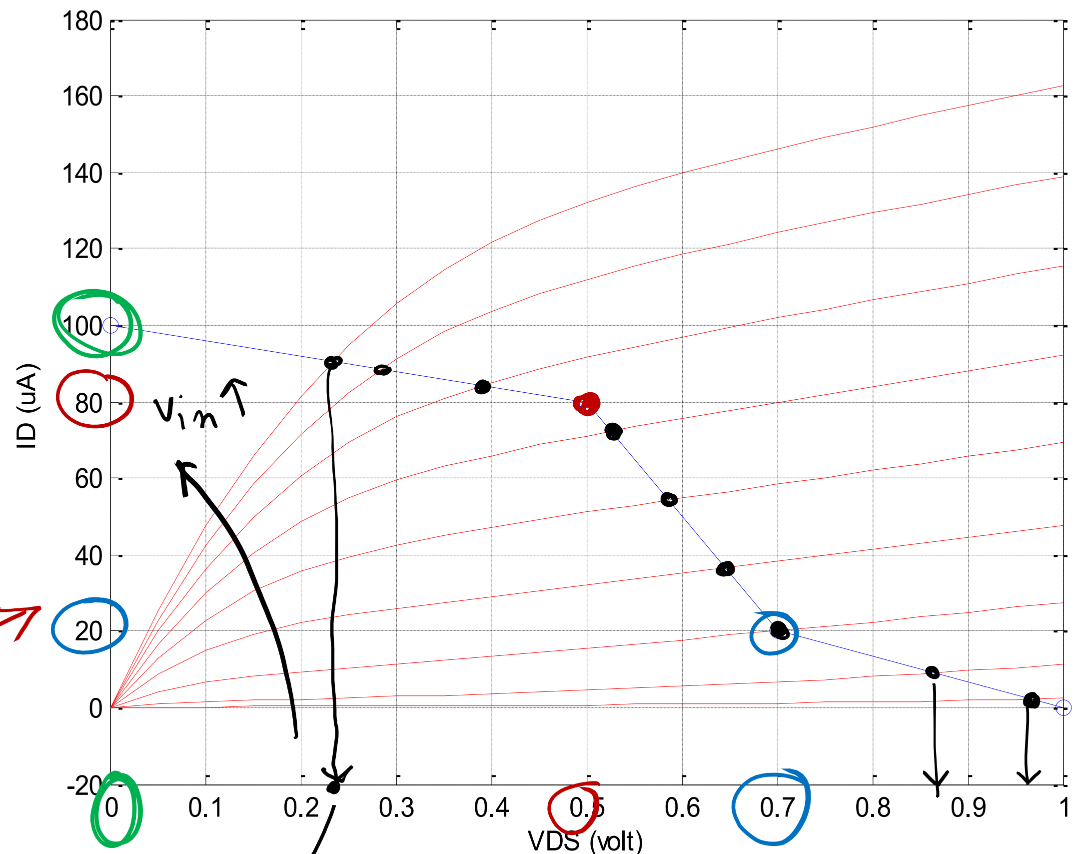


- **Strategy:**
  - Superimpose load I-V characteristic on top of NMOS I-V

Step 1: Coordinate Transform

- $V_{out} = V_{DS} = V_{DD} - V_{shaded\text{-}box}$





- Next, pick intersect points

Step 2: Intersect Points Form the VTC

Noise margin high:

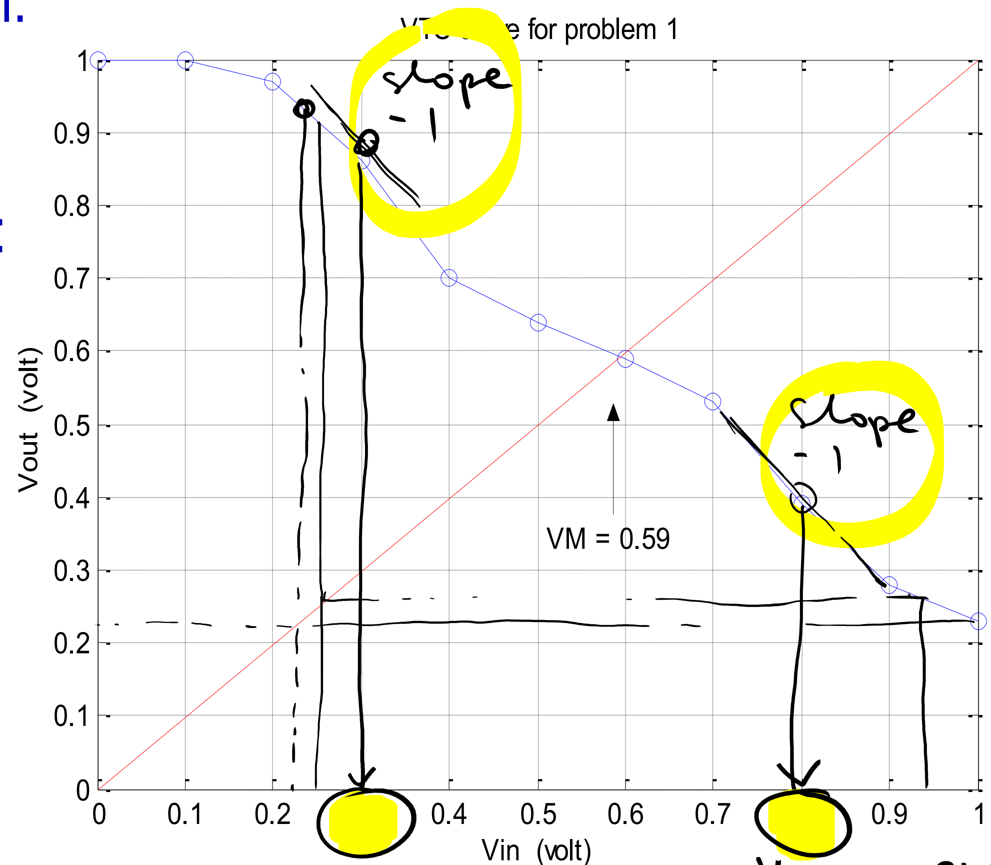
$NM_H = V_{OH} - V_{IH}$

Noise margin low:

$NM_L = V_{IL} - V_{OL}$

$NM_L \approx 0.05V$

$NM_H \approx 0.1V$



$V_{IL} \approx 0.3V$

$V_{IH} \approx 0.8V$

1) assume $V_{OH} = 1V$
$\Rightarrow V_{OL} \approx 0.25V$

2) iterate
$V_{OH} \approx 0.9V$

$\Downarrow$

$\boxed{V_{OH} \approx 0.9V \quad V_{OL} \approx 0.25V}$

$V_{OL} = f(V_{OH})$

$V_{OH} = f(V_{OL})$