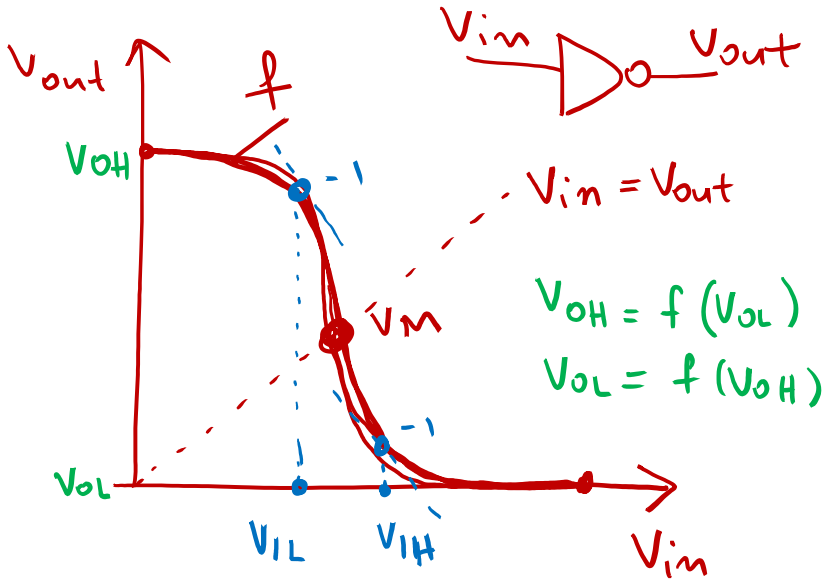
ECE115C – Digital Electronic Circuits

Lecture 5:

Propagation Delay

Four Key Design Metrics for Digital ICs

- Cost of ICs
- Reliability
- **Speed**
  - Logic delay (today)
  - Wire delay (next lecture)
- Power

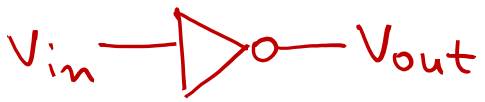


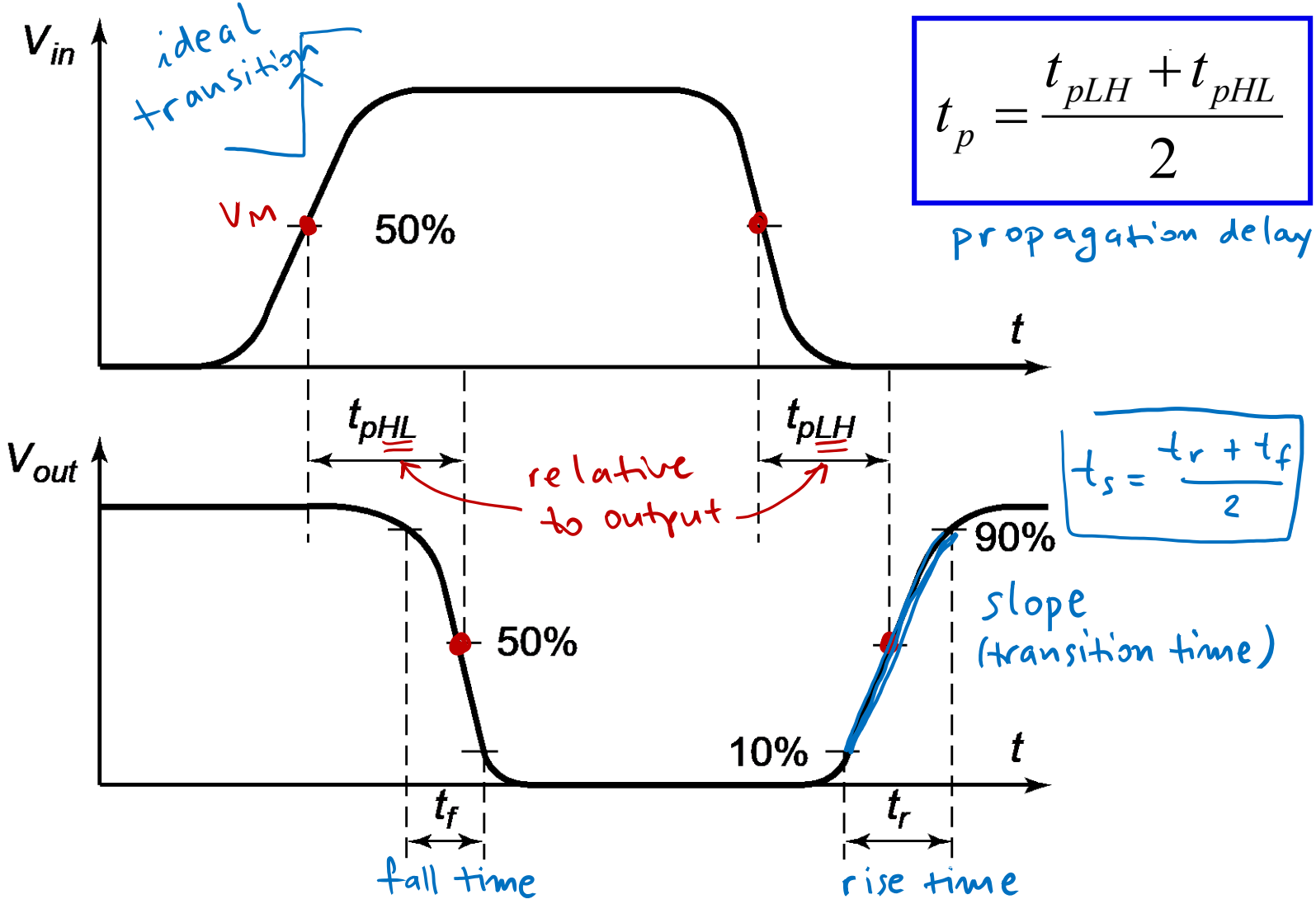
$NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$

[$|g| > 1$ necessary]

Performance: Delay Definitions



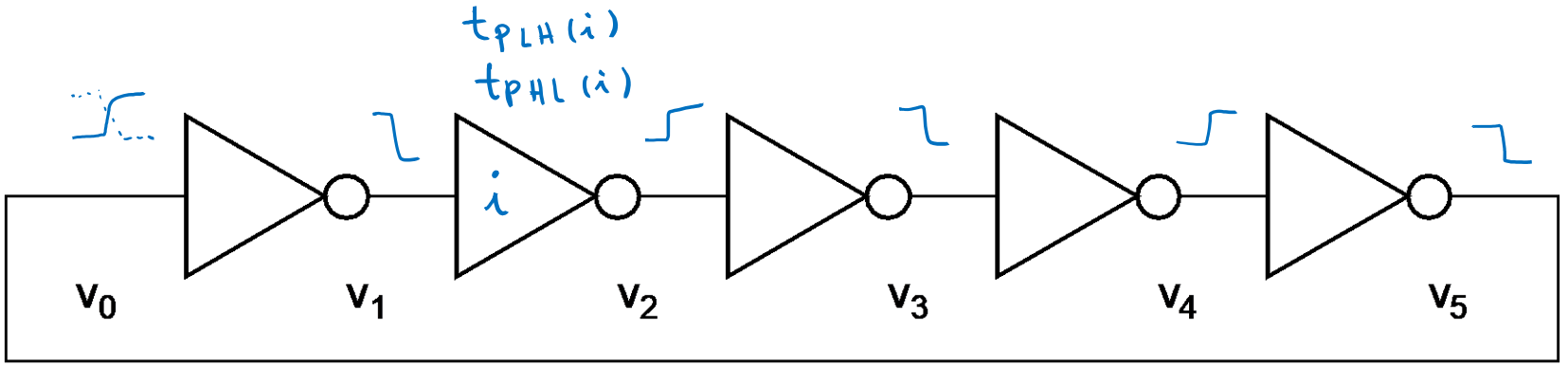


$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

propagation delay

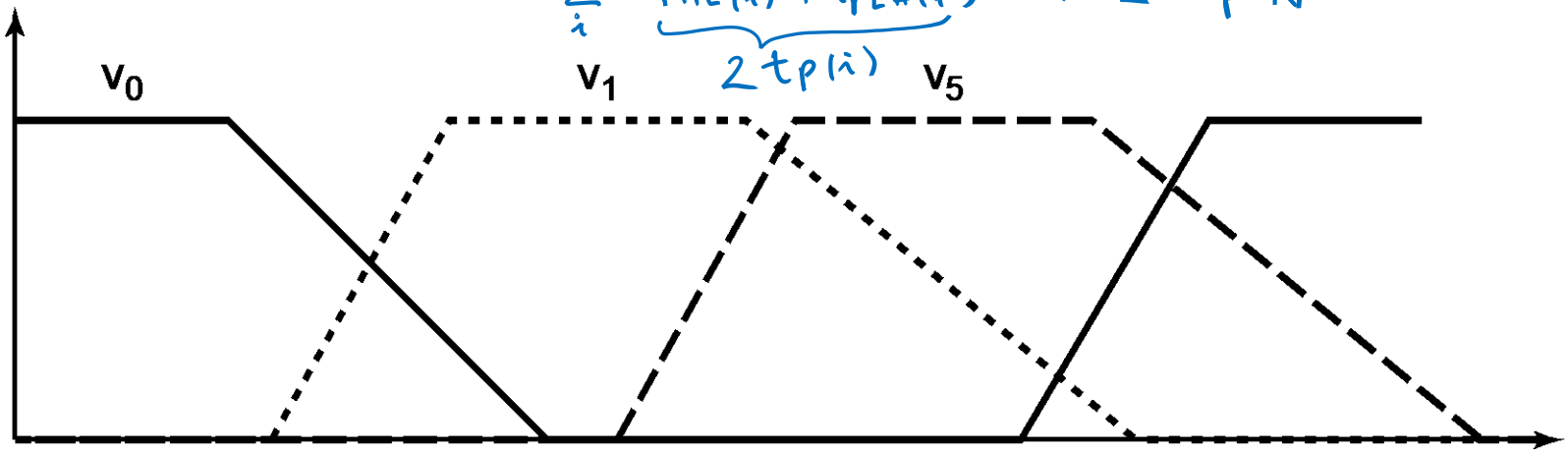
$$t_s = \frac{t_r + t_f}{2}$$

Technology Characterization: Ring Oscillator for t_p



$$T = \sum_i t_{pHL(i)} + t_{pLH(i)} \rightarrow 2\, t_p\, N$$

$2\, t_{p(i)}$



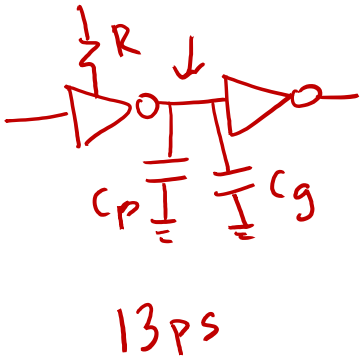
measure T by simulation

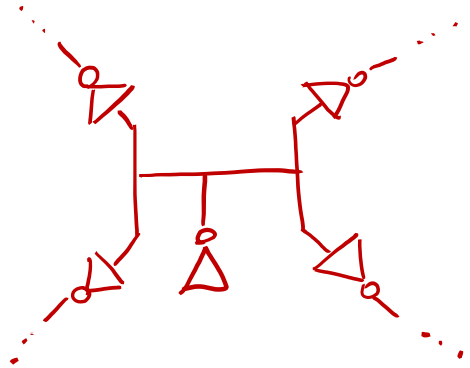
$$T = 2 \times t_p \times N$$

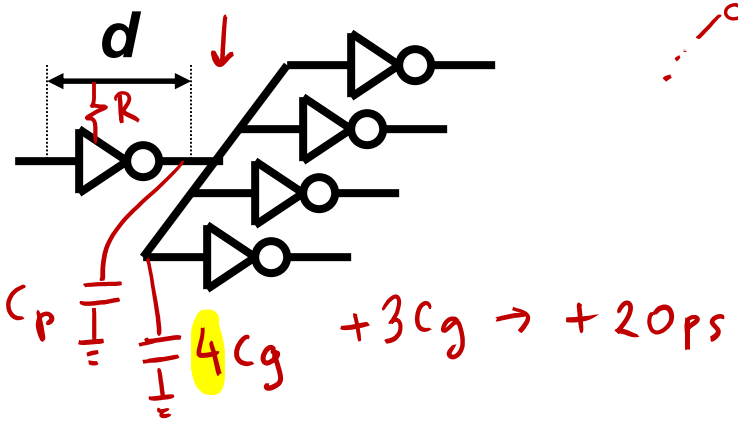
Tutorial 2: $t_p = 13ps$

Performance: FO4 Inverter

- Measures quality of design across different technology generations



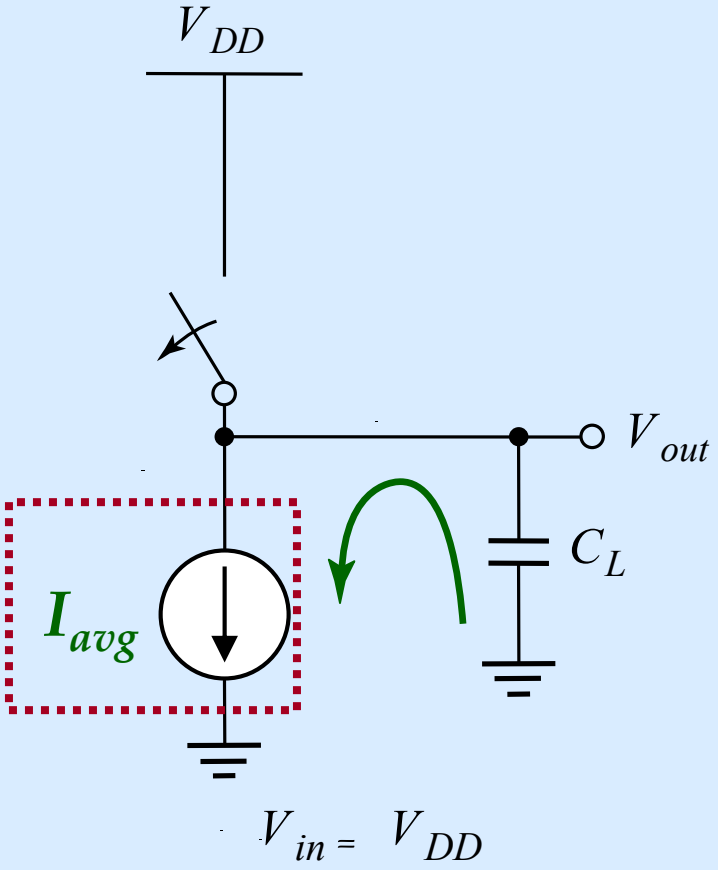




Tutorial 2: ***FO4 = 33ps***

CMOS Inverter Propagation Delay: Approach 1

MOS Current Model



$$t_{pHL} = \frac{C_L \cdot V_{swing}/2}{I_{avg}}$$

out: "1" → "0"

reduce delay by:

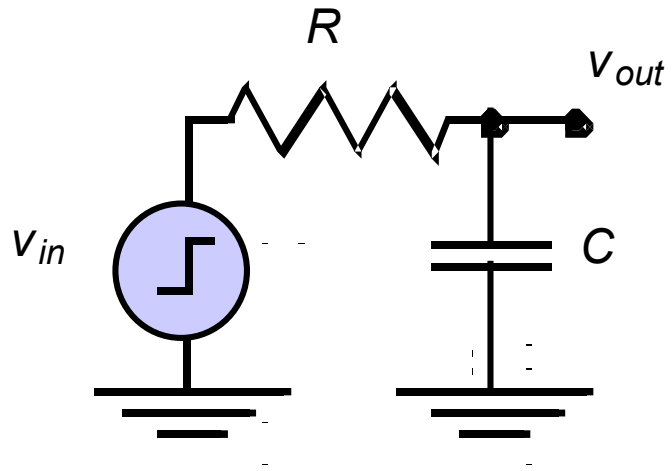
#1: reduce cap

$$t_{pHL} \sim \frac{C_L}{k_n \cdot V_{DD}}$$

#3: increase voltage

#2: increase $\frac{W}{L}$ (factors into C_L)

A First-Order RC Network: Step Response



Step response:

$$v_{out}(t) = \left(1 - e^{-t/\tau}\right) \cdot v_{in}$$

① $v_{out}(0) = V_0$

② $v_{out}(\infty) = V_\infty$

$V_0, V_\infty \in \{V_{OL}, V_{OH}\}$

Switching pt: $v_{out}(t_{pHL}^{pLH}) = V_M$

$\tau = RC$

$t=\infty: e^{-t/\tau} = 0$

$$v_{out}(t) = V_\infty + (V_0 - V_\infty)\, e^{-t/\tau}$$

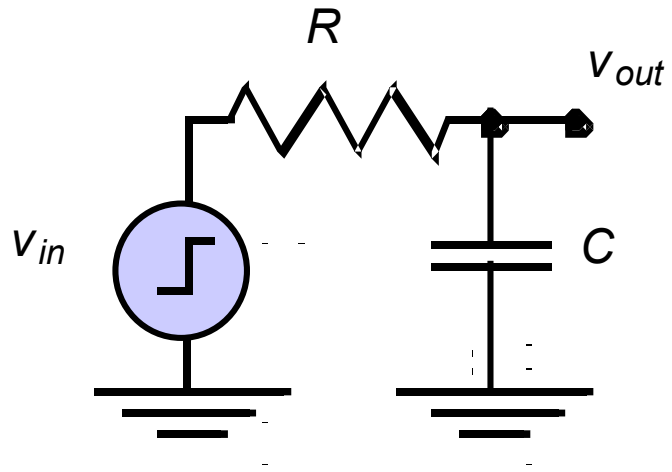
GENERAL FORMULA

① $t=0: e^{-t/\tau} = 1$

special case: $V_\infty = V_{DD}$ & $V_0 = 0$

↳ $v_{out}(t) = V_{DD}\left(1 - e^{-t/\tau}\right)$

A First-Order RC Network: Propagation Delay



Propagation delay:

$$t_p = \tau \cdot ln2 = 0.69RC$$ ✓

$t_s \sim 2.2\ RC$ slope 90% point

$v_{out}(t) = V_\infty + (V_0 - V_\infty)\, e^{-t/\tau}$

$v_{out}(t_p) = V_M$

$V_M = V_\infty + (V_0 - V_\infty)\, e^{-t_p/\tau}$

$$t_p = \tau \ln \frac{V_0 - V_\infty}{V_M - V_\infty}$$ GENERAL

special case:

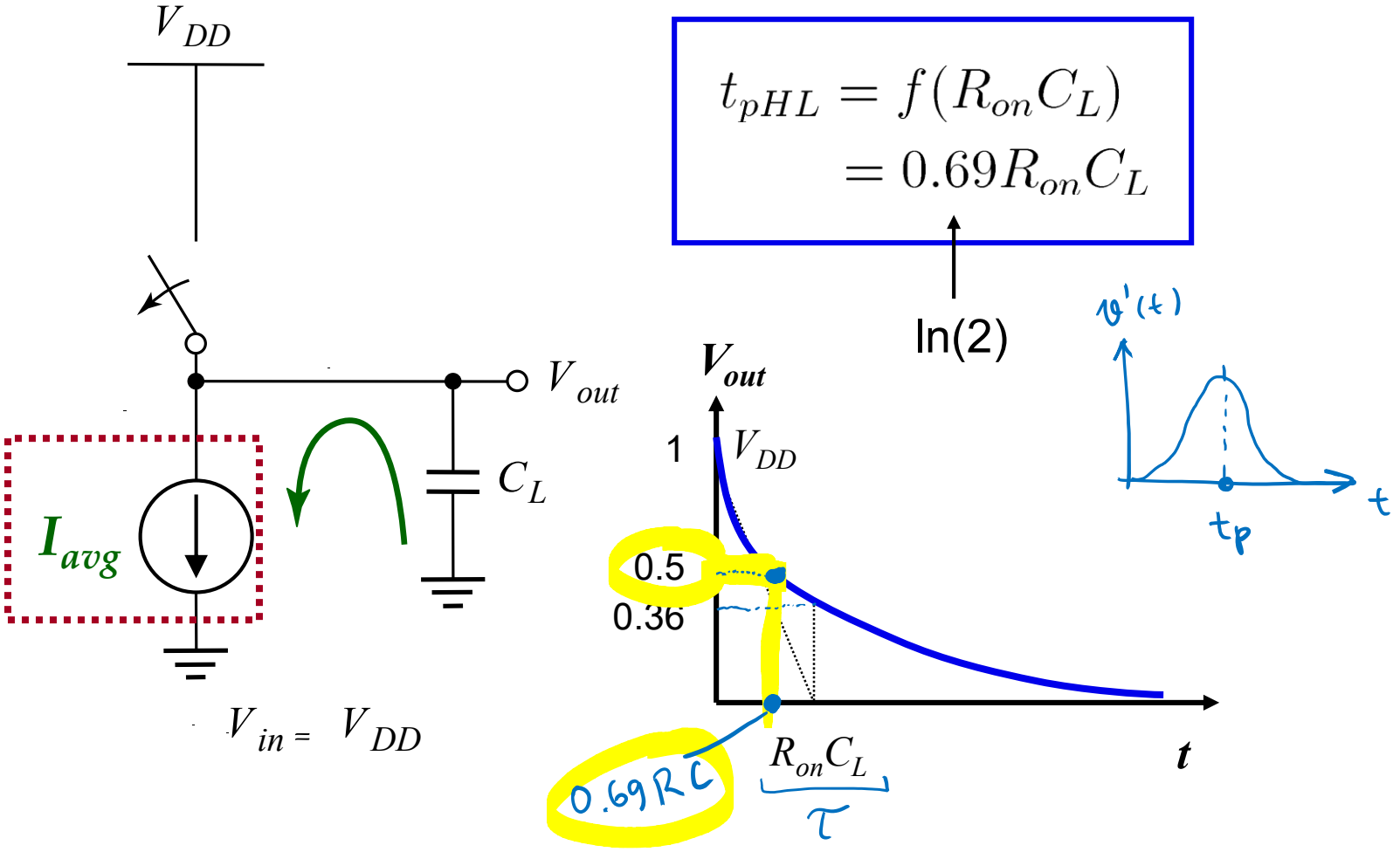
$V_M = \frac{V_{DD}}{2}$

$V_0 = 0,\ V_\infty = V_{DD}$

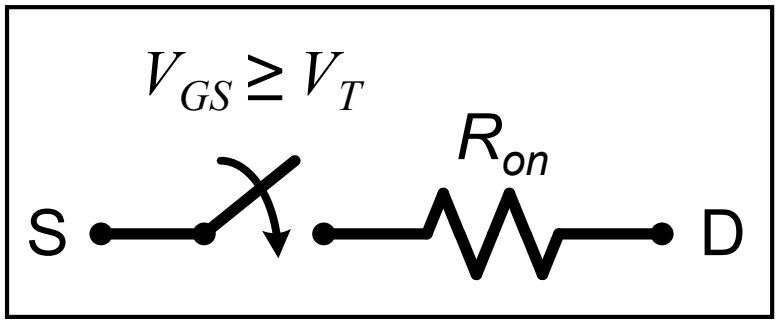
$$t_p = \tau \ln \frac{-V_{DD}}{-V_{DD}/2} = \tau \ln 2 = 0.69\ RC$$

CMOS Inverter Propagation Delay: Approach 2

MOS Resistance Model

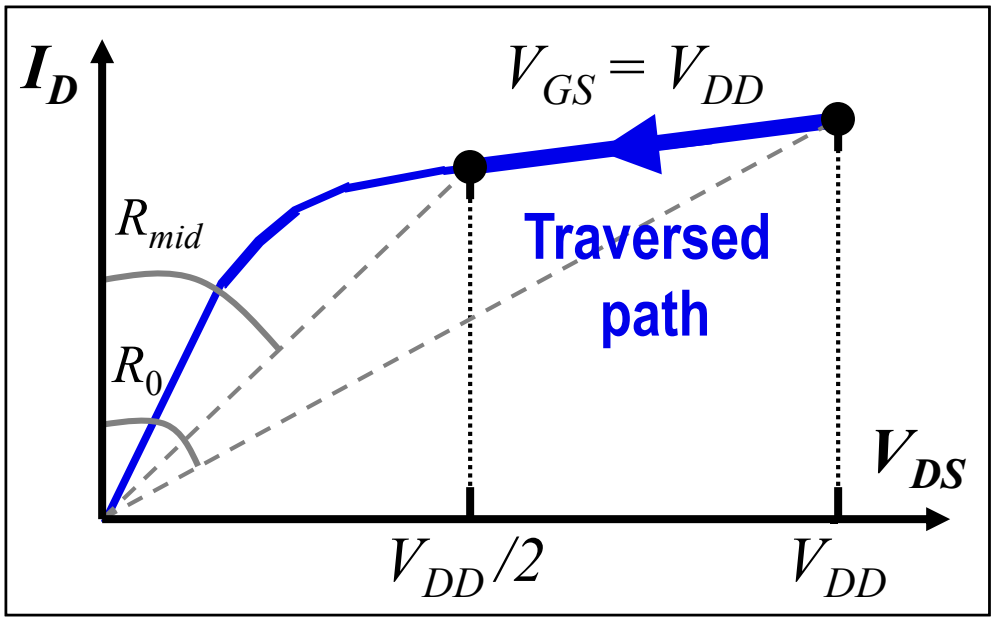


Review: Transistor as a Switch



$$R_{on} \approx \frac{1}{2}(R_0 + R_{mid})$$

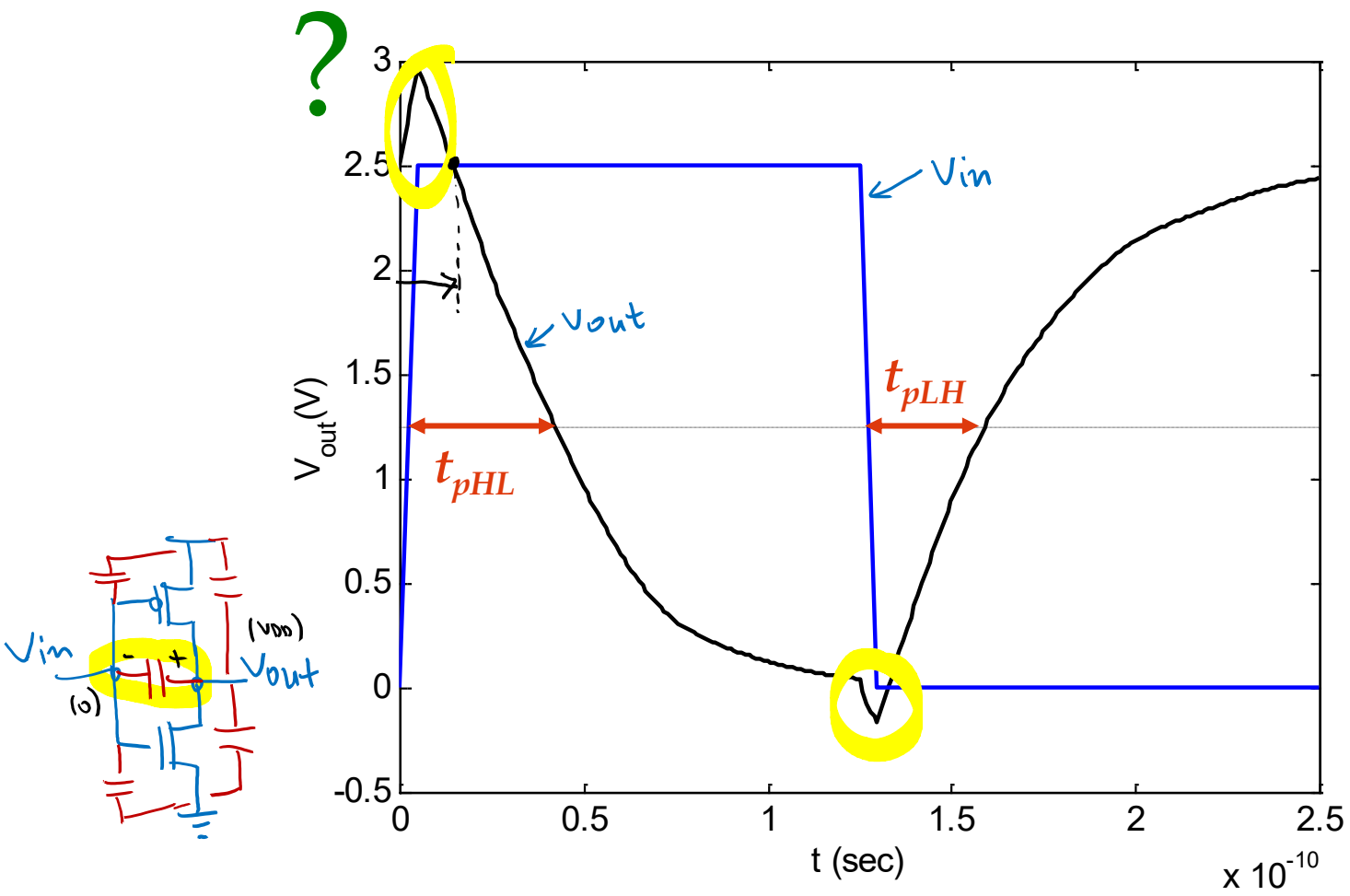
good approximation (I-V ≈ linear)



$$R_{on} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT} \cdot (1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT} \cdot (1 + \lambda V_{DD}/2)}\right)$$

$$R_{on} \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)$$

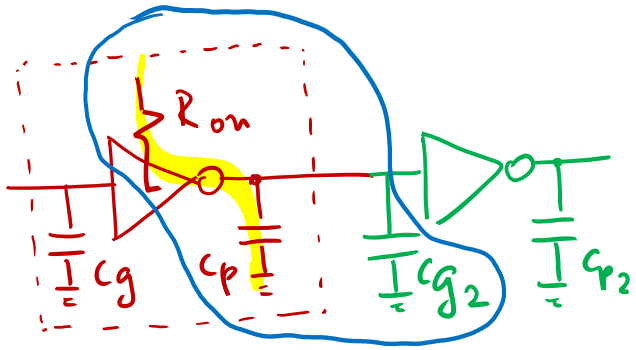
Transient Response



Design for Performance

- **Keep capacitances small**
- **Increase transistor sizes**
  - watch out for self-loading!
- **Increase V_{DD} (?)**

$$t_{pHL} \sim \frac{C_L}{k_n \cdot V_{DD}}$$

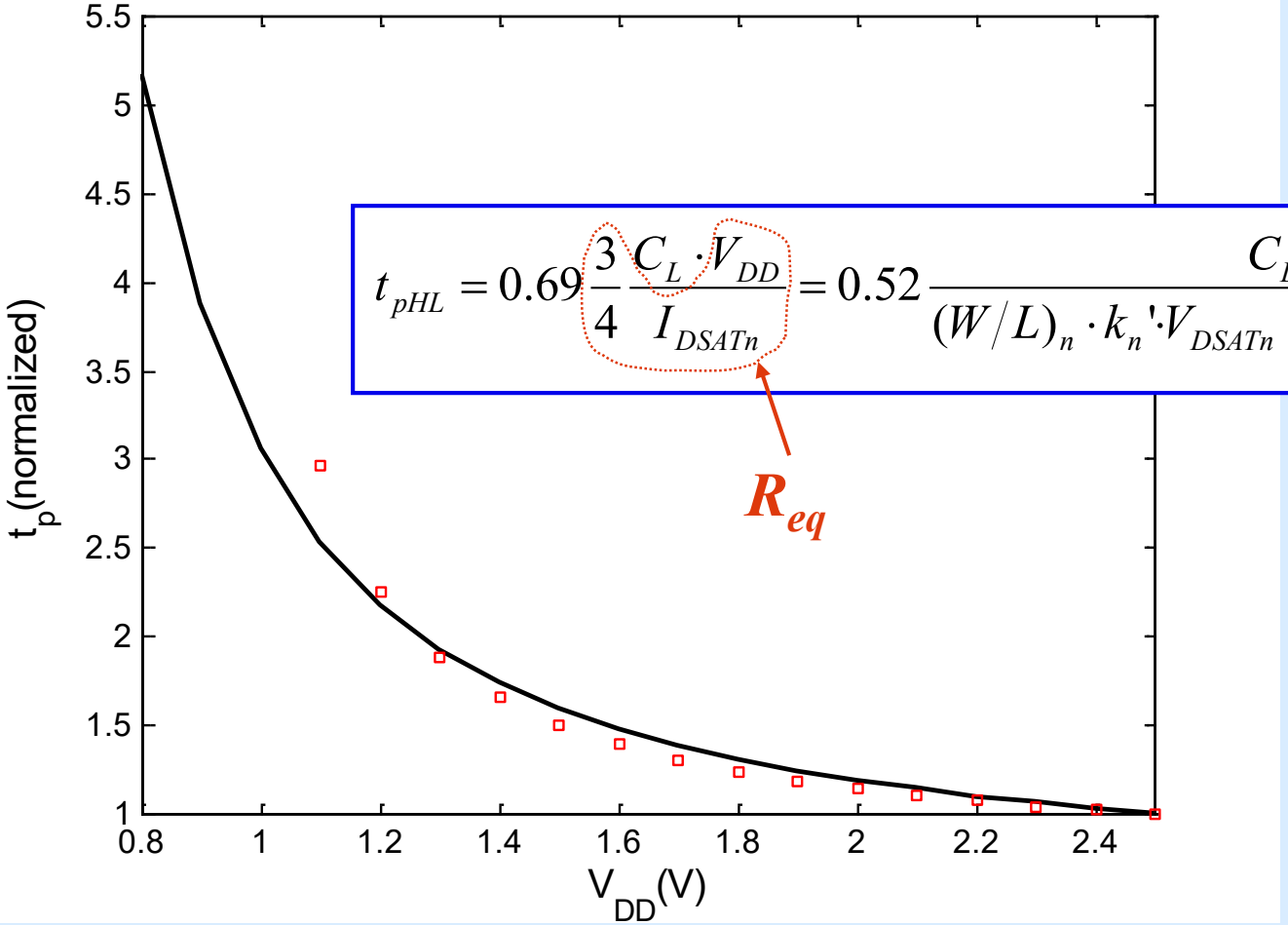


$R_{on} \sim \frac{1}{W}$

$C_p, C_g \sim W$

$R_{on} \cdot C_p \sim \frac{1}{W} \cdot W =$ constant

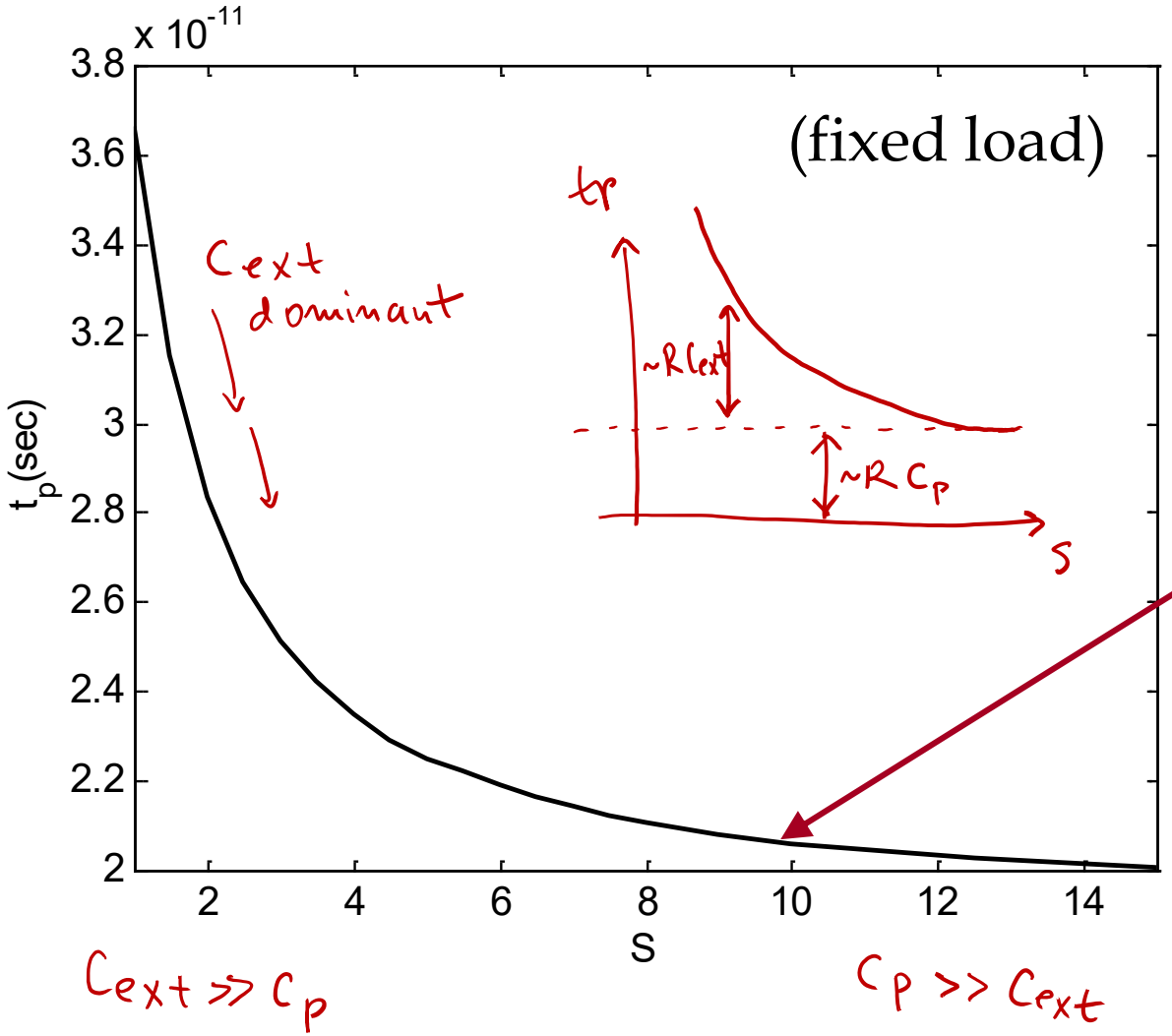
Delay as a function of V_{DD}

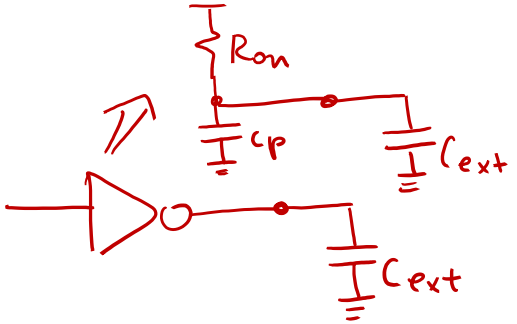


$$t_{pHL} = 0.69 \frac{3}{4} \frac{C_L \cdot V_{DD}}{I_{DSATn}} = 0.52 \frac{C_L \cdot V_{DD}}{(W/L)_n \cdot k_n' \cdot V_{DSATn} \cdot (V_{DD} - V_{Tn} - V_{DSATn}/2)}$$

R_{eq}

Device Sizing





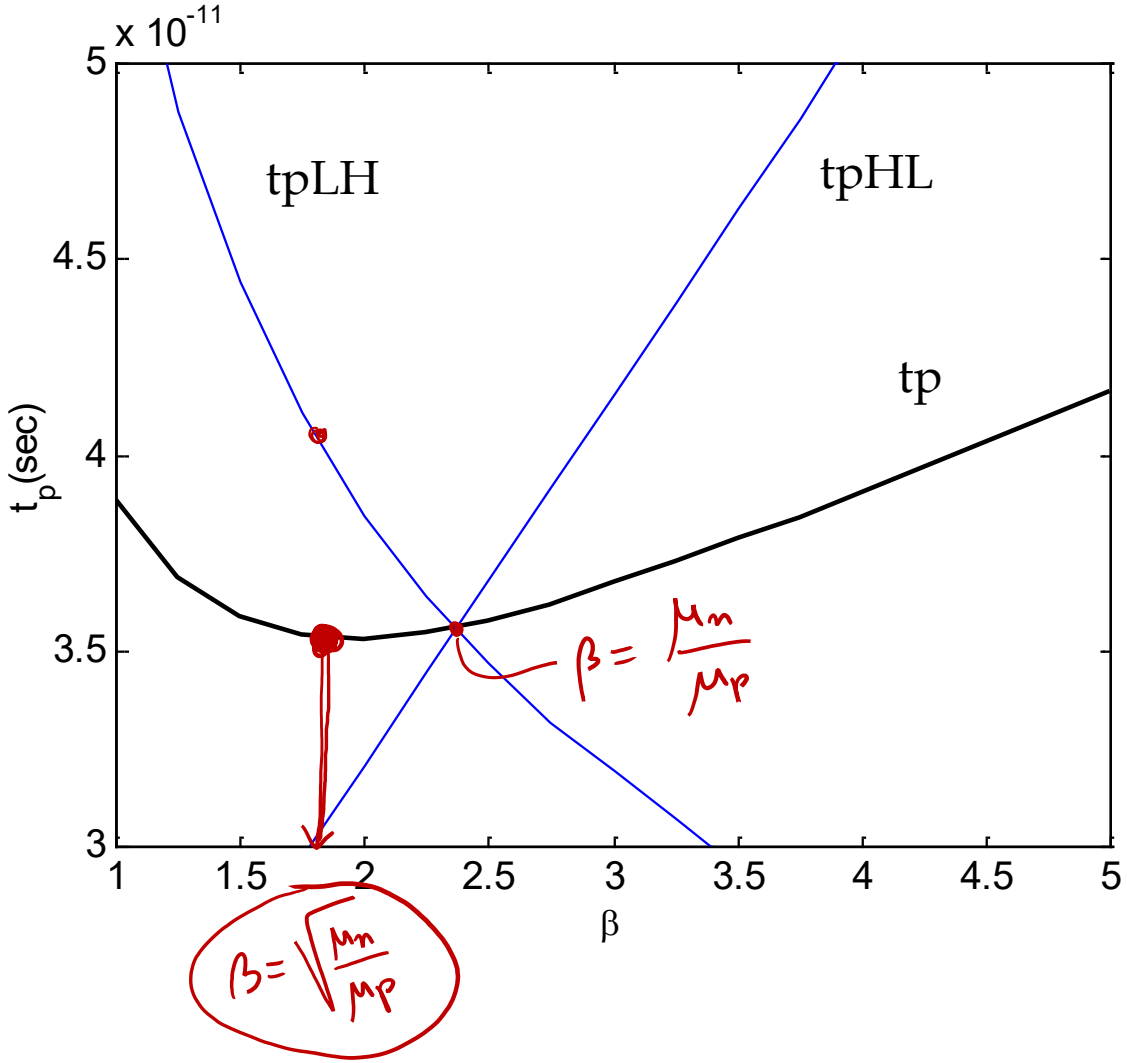
Self-loading effect: Intrinsic capacitances dominate

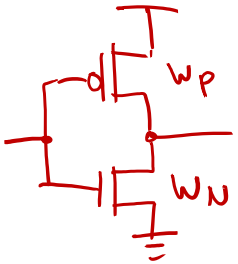
$W \rightarrow S \cdot W \uparrow$

$R \sim \frac{1}{S} \downarrow$

$C_p \sim S \uparrow$

NMOS/PMOS Ratio



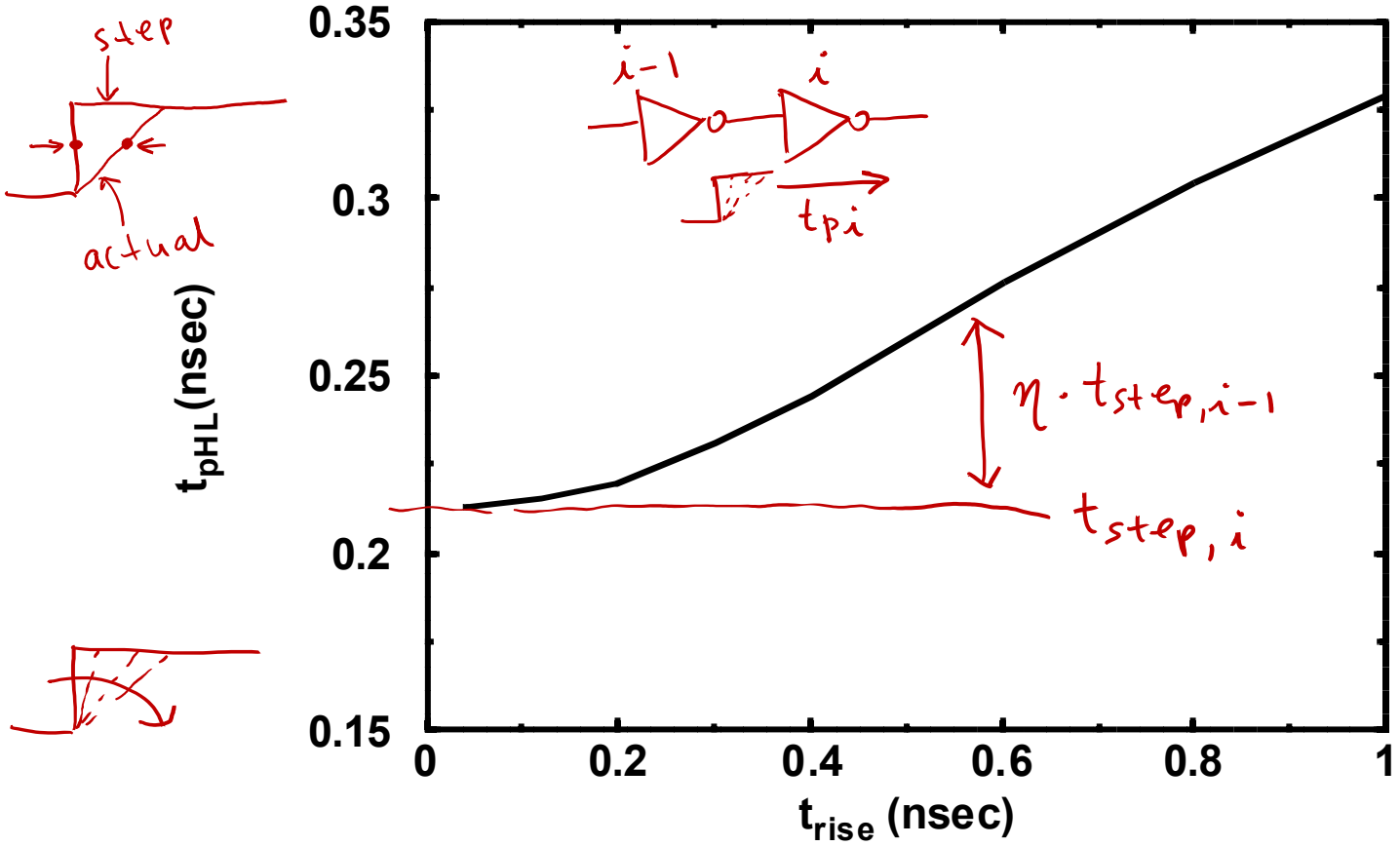


$$\beta = W_p / W_n$$

typical std-cell lib:

$\frac{W_p}{W_N} \approx 1.3 - 1.7$

Impact of Rise Time on Delay

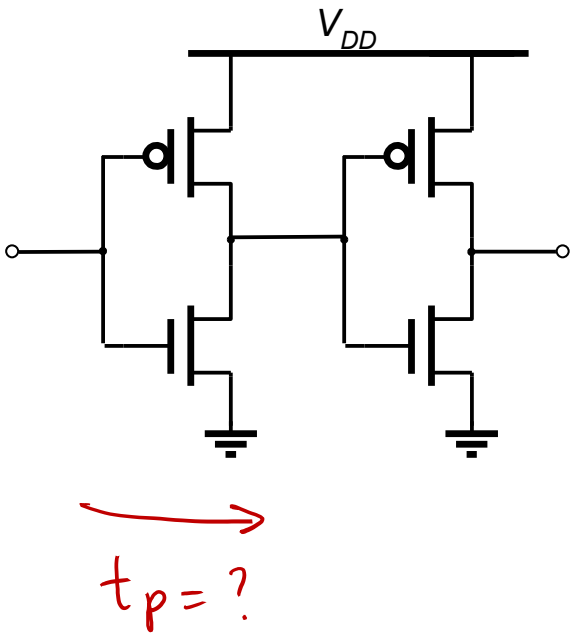


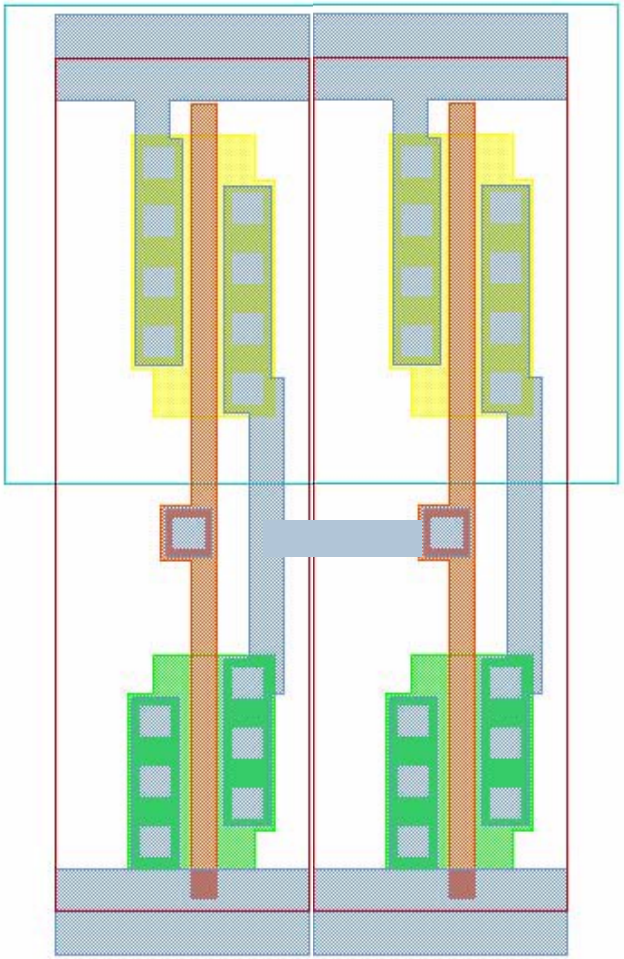
$$t_p = t_{step(i)} + \eta \cdot t_{step(i-1)}$$

$t_p \sim 0.69RC$

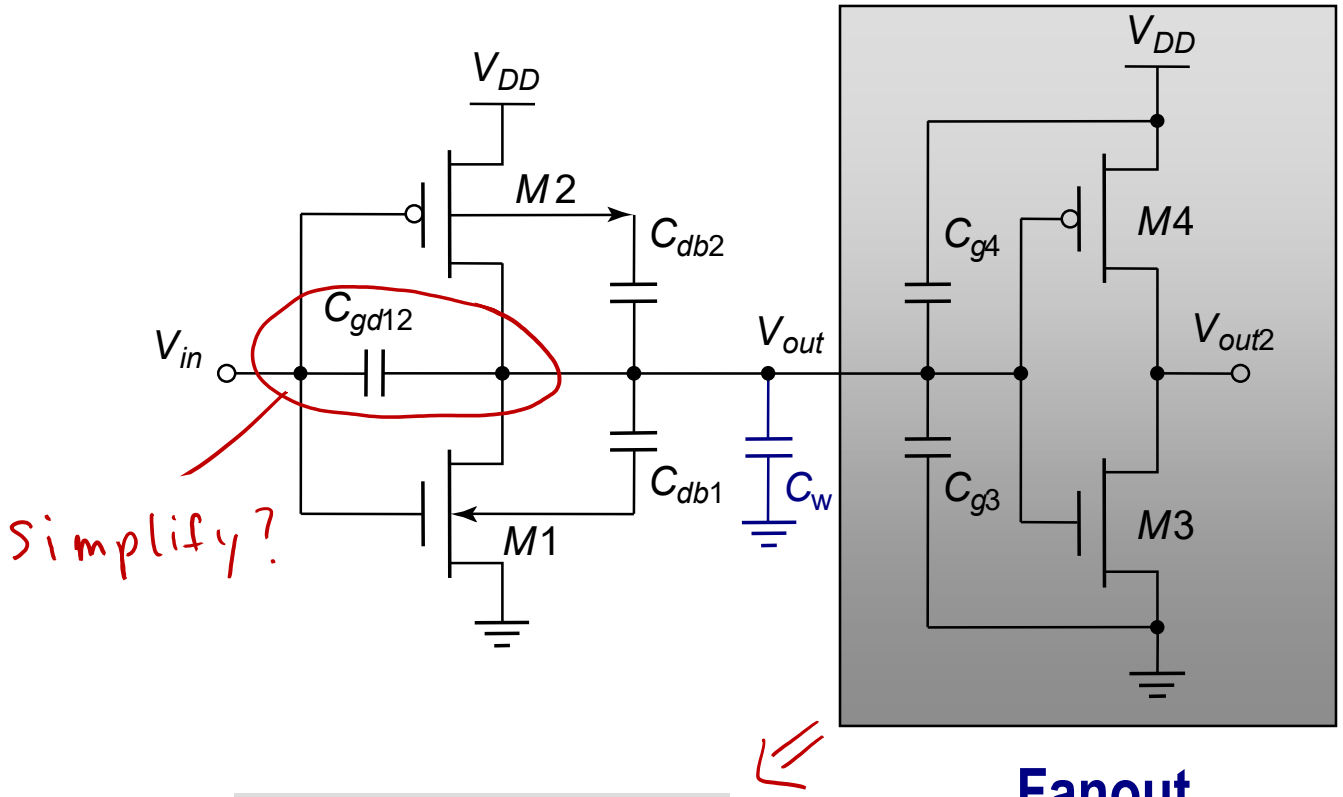
$t_s \sim 2.2RC$

Two Inverters

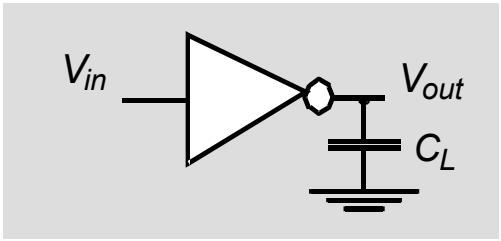




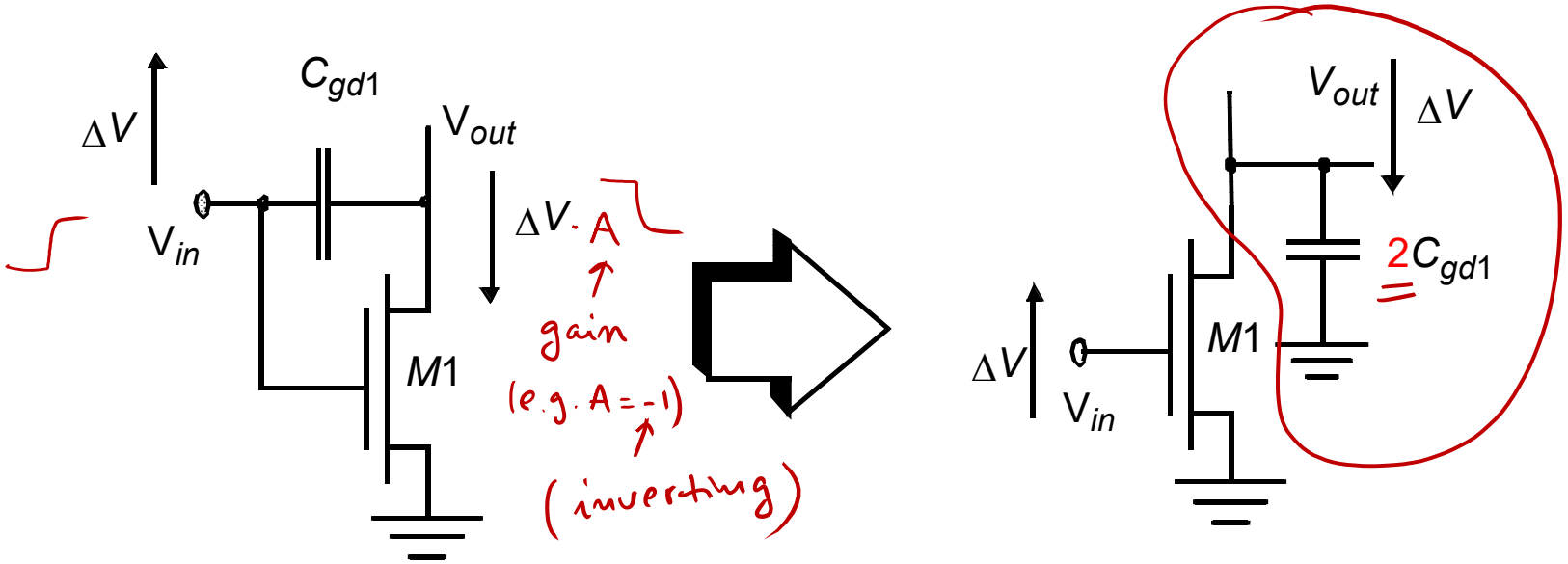
Computing the Capacitances



Simplified Model



The Miller Effect



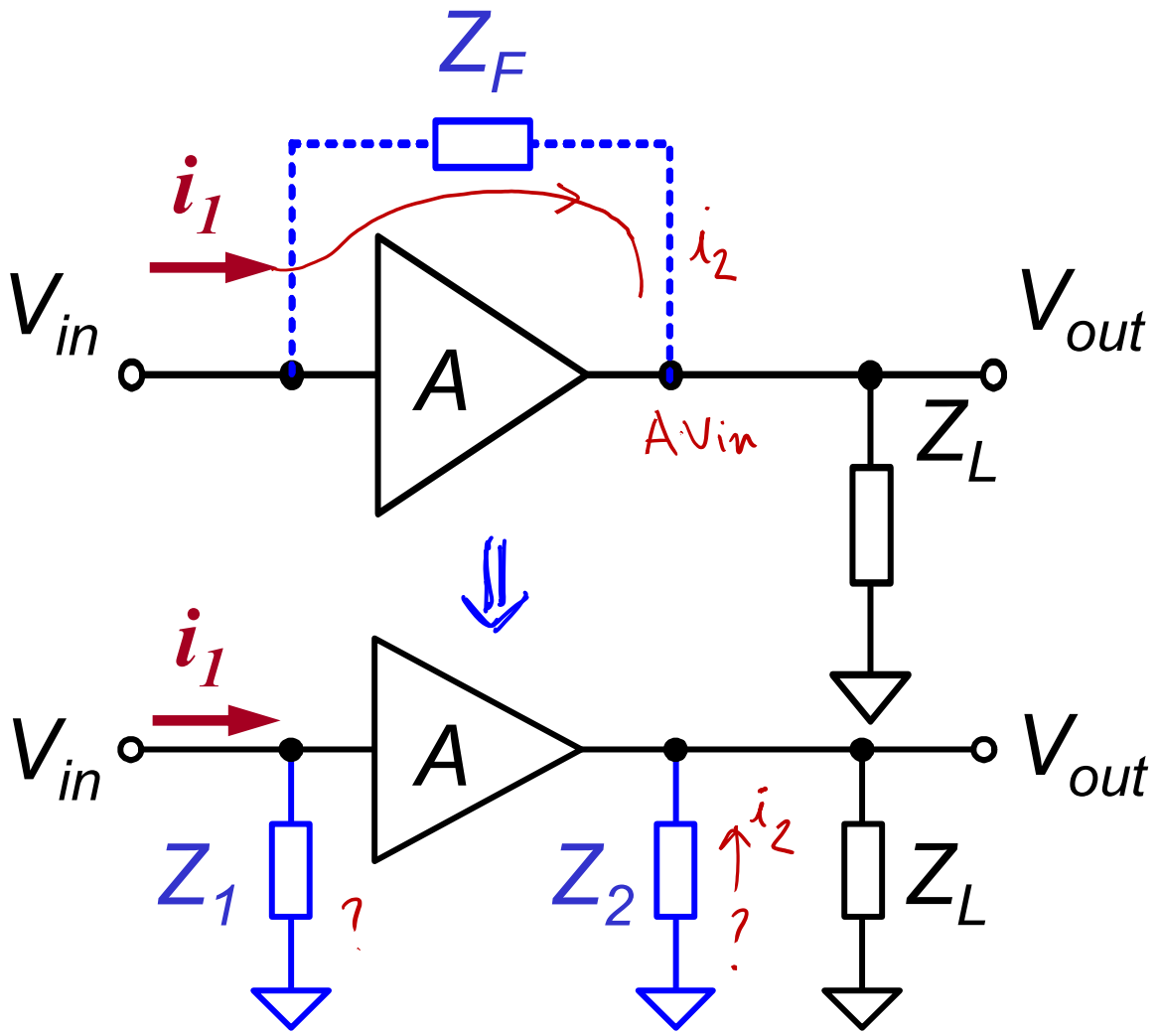
"A capacitor experiencing identical but opposite voltage swing at both terminals can be replaced by a capacitor to ground, whose value is two times the original value"

Miller Effect

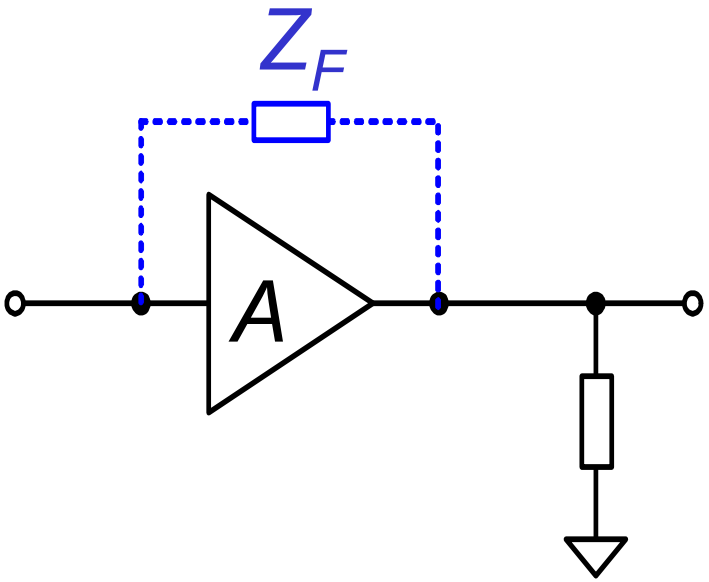
$$i_1 = \frac{V_{in}(1-A)}{Z_F}$$

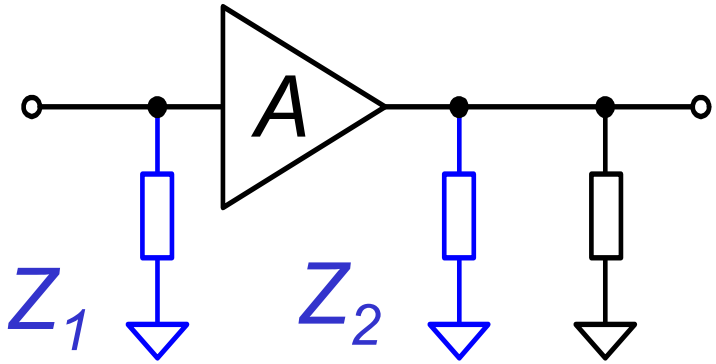
$$Z_1 = \frac{Z_F}{1-A}$$

$$i_1 = \frac{V_{in}}{Z_1}$$



Miller Effect





$$Z_1 = \frac{Z_F}{1 - A}$$

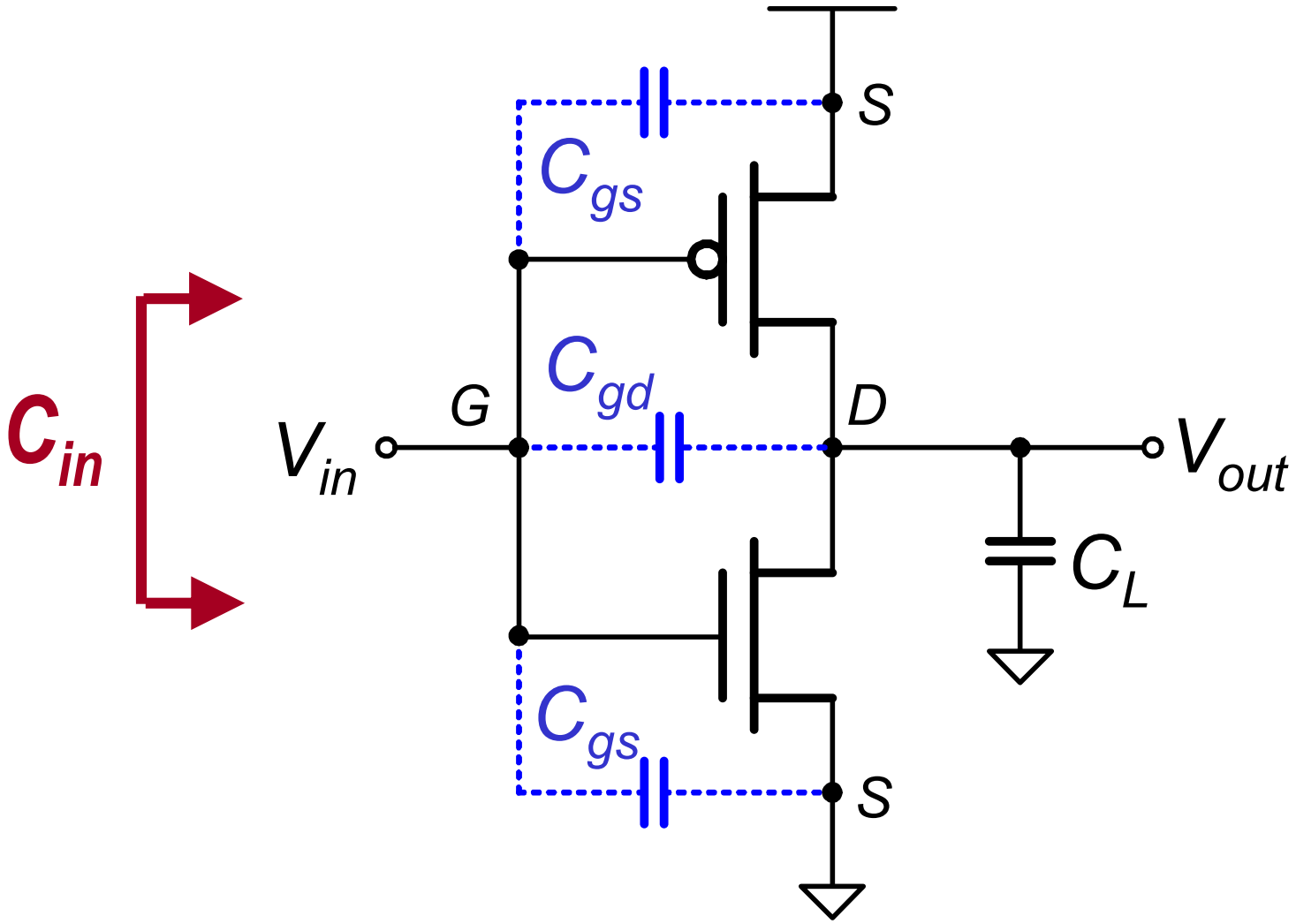
$$Z_2 = \frac{Z_F}{1 - \frac{1}{A}}$$

$Z \sim \frac{1}{j\omega C}$

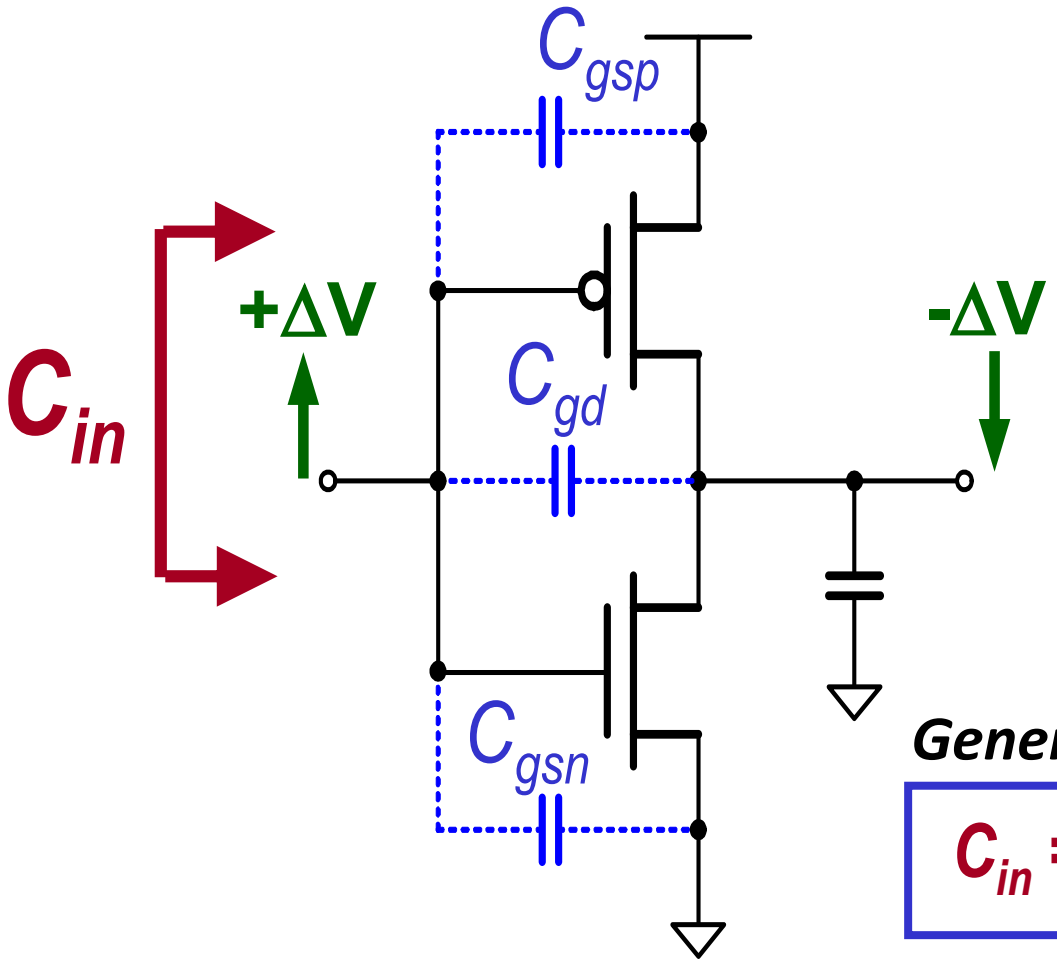
$C_1 = C_F \cdot (1 - A)$

$C_2 = C_F \cdot (1 - 1/A)$

The CMOS Inverter: C_{in}



CMOS Inverter Example: C_{in}



$$C_{gs} = C_{gsn} + C_{gsp}$$

$$C_{gd} = C_{gdn} + C_{gdp}$$

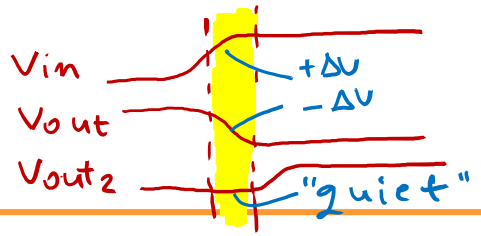
$$A = -1$$

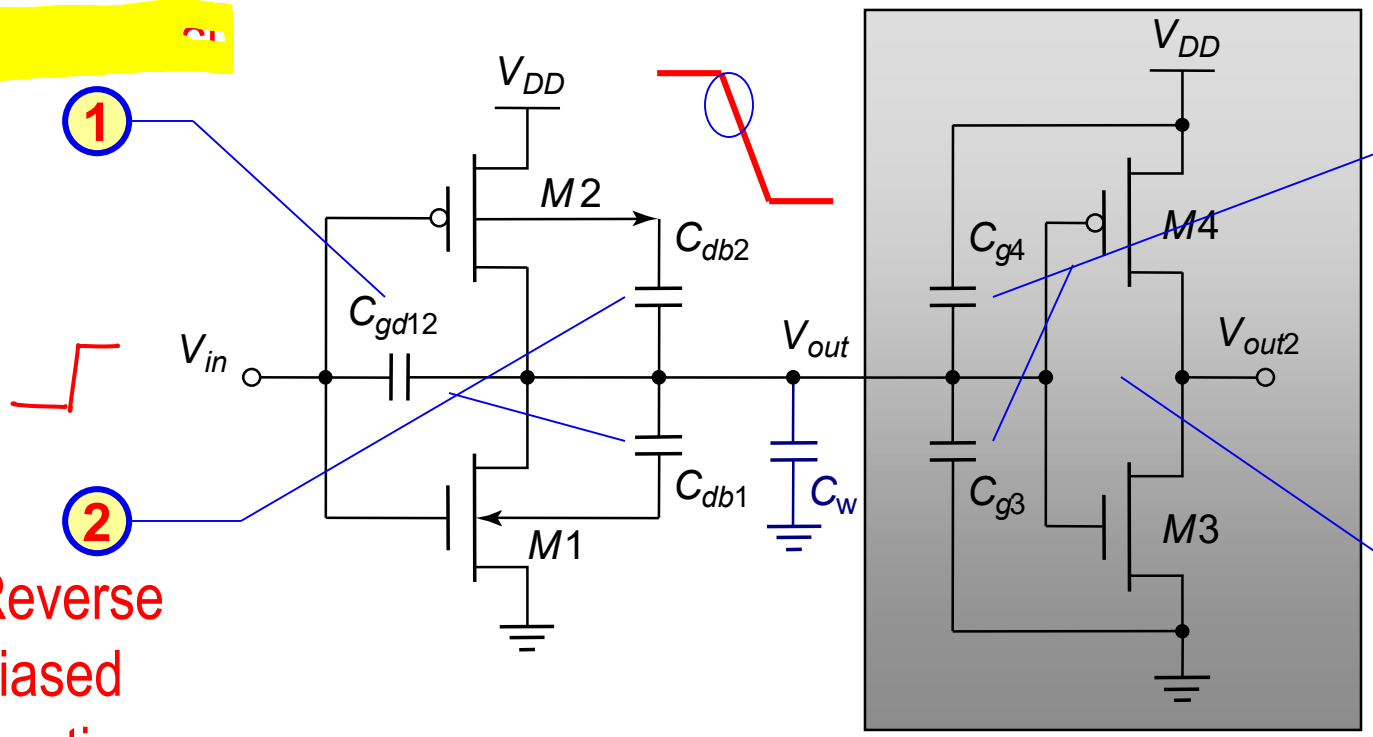
General formula:

$$C_{in} = C_{gs} + C_{gd}(1 - A)$$

Approximation for CMOS gates: $C_{in} = C_{gs} + 2C_{gd}$

Computing the Capacitances





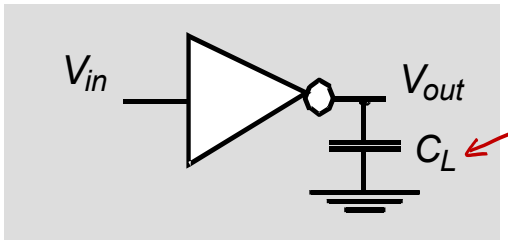
Reverse biased junction

Off → Sat (M_4)

Lin (M_3)

No Miller effect

Simplified Model



Fanout

$$C_L = \overbrace{C_w + C_{g3} + C_{g4}}^{C_{ext}} + \overbrace{C_{db1} + C_{db2}}^{C_{par}} + 2(C_{gd1} + C_{gd2})$$

Miller factor

Computing the Capacitances

1 Miller effect

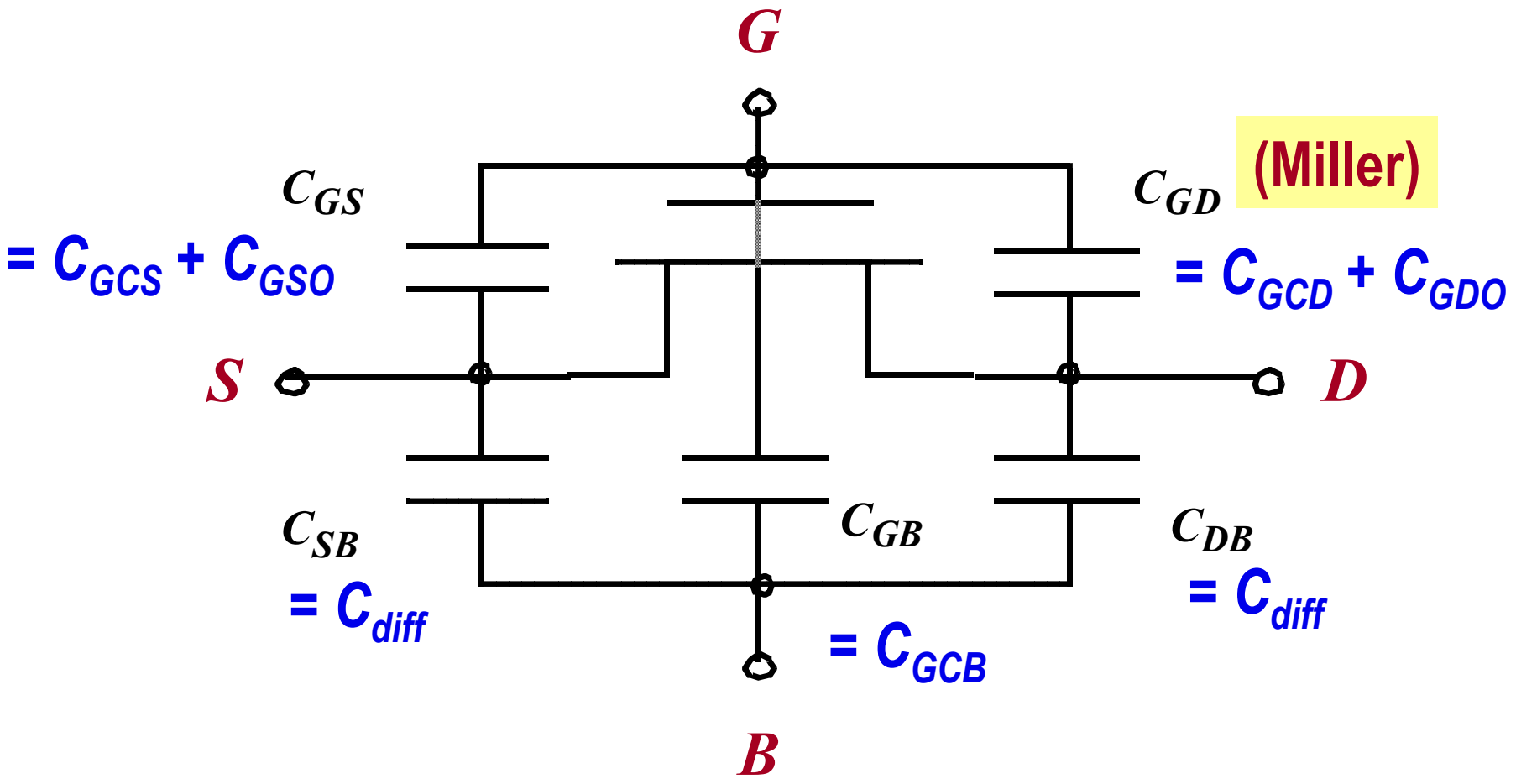
2 Reverse biased junction

Capacitor	Expression
C_{gd1}	CGD0 W_n
C_{gd2}	CGD0 W_p
C_{db1}	K_{eqn} (AD_n CJ + PD_n CJSW)
C_{db2}	K_{eqp} (AD_p CJ + PD_p CJSW)
C_{g3}	C_{ox} W_n L_n (Off → Sat*)
C_{g4}	C_{ox} W_p L_p (Lin*)
C_w	From Extraction
C_L	Σ

3

* assuming LH transition at V_{out}

Capacitive Device Model For Circuit Analysis



Simplified Macro Model

- **Consider two macro capacitances**
  - Input gate capacitance, C_{in} (or C_{gate})
  - Output parasitic (self-loading capacitance), C_{par}
- **Assume that both capacitances are linearized**
  - C_{in} and C_{par} are proportional to W
    (remember, we keep L at L_{min}, so it is lumped into constant)
  - In our 90nm technology, C_{par} / C_{in} is about 0.6
- **For gate delay analysis, we will use:**

$$C_{in} = 2fF/\mu m \qquad C_{par}/C_{in} = 0.61$$