EEM216A Design of VLSI Circuits and Systems **Fall 2023**
Prof. Dejan Marković Homework #1

Due: **Wed, 10/18, 11:59pm**
Submissions to be uploaded in Gradescope

Problem 1: MOS Model Extraction

In this question you will calculate the effective input capacitance, effective parasitic capacitance and the effective resistance of an inverter using the Cadence simulation environment.

Using Cadence Virtuoso, create the model inverter using the n105 and p105 NMOS and PMOS models as outlined in the previously distributed "Running Synopsys 32/28nm Generic Library Simulations in Cadence 6.1.4" tutorial. Enter the following parameters for the sizing and supplies of the transistors.

$(W/L)_n$ = 100nm/32nm, $(W/L)_p$ = 200nm/32nm
V_{DD} = 0.8V, V_{SS} = 0V

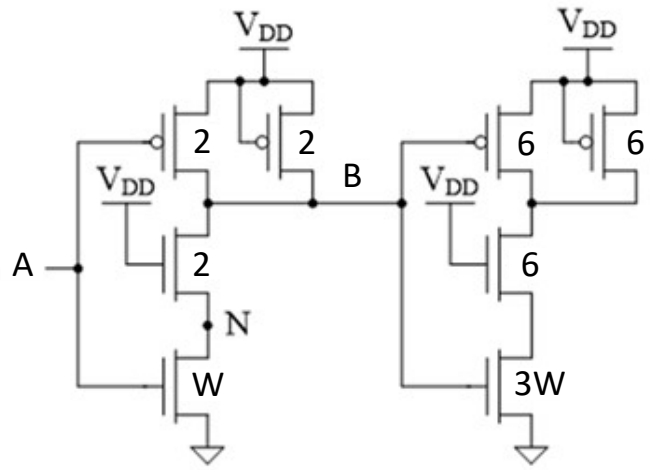
a. Using this inverter, create the design on slide 3.12. Adjust the C_gate capacitance till the delays of t_pHL match. Record this value. Do the same for t_pLH. Take the average which will be your C_gate.
b. Find out a reasonable way to determine C_parasitic (Hint: you can use slide 3.13). Describe the methodology you used, perform the required simulation and record the result.
c. Use the setup in Slide 3.14 to find out R_eff of the transistor.

Remember to take snapshots of your Cadence setup for each part, and any other simulation result you think is worth mentioning.

(Please follow the instructions on CCLE (File: Running Synopsys 32/28nm Generic Library Simulations in Cadence) to get familiar with tool setup)

Problem 2: Delay Calculation

Assume that $C_{S/D}$ =0.5C_0 fF/ µm, C_{gate}=C_0 fF/ µm, R_N=R_0 kΩ-µm, V_{DD}=1V. All numbers in the figure are in microns.



a. Assume no sharing of source/drain (S/D) of a transistor. Find the propagation delay expressed in the given variables and width W that minimizes the delay of the gate from input A's rising edge to output B's falling edge. Consider the internal capacitance of the gate.

T_p=
W_{opt}=

b. If sharing of S/D capacitance is applied, with a fingered layout that uses a W=2 finger width, does the optimum W from (a) increase or decrease (circle one answer)? What are the capacitances of nodes B and N at this new optimal?

W_{opt}: increase / decrease
C_B=
C_N=

Problem 3: Gate Propagation Delay

For this question you can ignore body effect and channel length modulation. Equivalent resistance R_{eq} (W/L = 1) of NMOS and PMOS transistors are R_n = 10kΩ and R_p = 25kΩ, respectively.

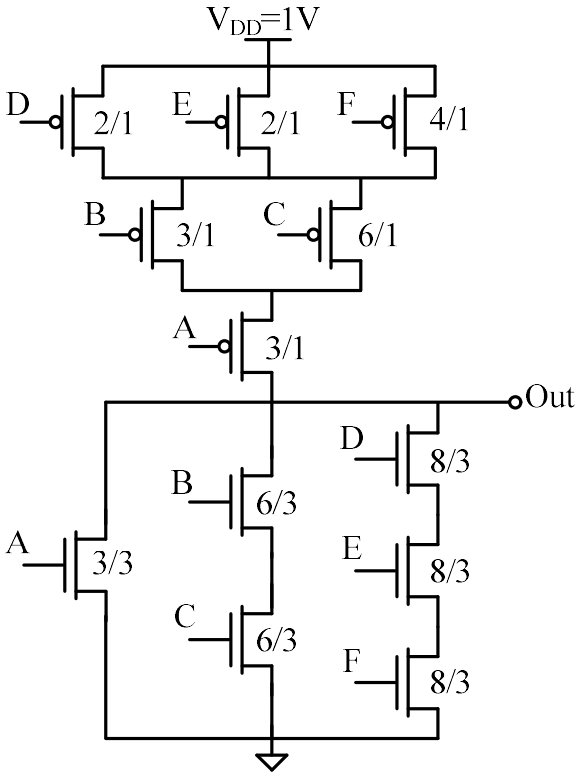


Figure 3

(a) What function is implemented by this circuit?

Out =

(b) Calculate the **worst-case** low-to-high propagation delay. Assume that all output capacitances are lumped together into a single load capacitance C_L = 45fF.
You may ignore all intermediate (internal) capacitances for this part.

Worst t_{pLH} =

(c) Calculate the **fastest** high-to-low propagation delay. C_L = 45fF.
You may ignore all intermediate (internal) capacitances for this part.

Best t_{pHL} =

(d) What are the input patterns that give the **worst-case t_{pHL}** and **t_{pLH}**. State clearly what the initial input patterns are and which input(s) has to make a transition in order to achieve this maximum propagation delay.
Consider the effect of the capacitances at the internal nodes for part (d).

	Worst-case t_{pHL}	**Worst-case t_{pLH}**
Input Pattern		