Running Synopsys 32/28nm Generic Library Simulations in Cadence 6.1.4

Tutorial

Vahagn Hokhikyan

Department of Electrical Engineering

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Purpose

Although in EE216A you will be working with the digital flow most of the time, there will be times when you will be asked to run simple analog simulations to do the lecture mini-assignments or to complete your homework problems. The Synopsys 32/28nm Generic Library standard cells analog simulation models are not available in a format readable by Cadence Virtuoso. The HSPICE version is provided instead. HSPICE simulations need to be run in command-line and are not user-friendly. Since focusing on the analog simulation tools is beyond the scope of this class, the following workaround for using Cadence Virtuoso is suggested for homework purposes. You are still free to use the HSPICE to run Synopsys 32/28nm Generic Library standard-cell simulations, however we will not have an assignment that requires this.

Assumptions

This tutorial assumes that you are familiar with the Cadence flow and followed the tool setup section outlined in the course wiki and have access to the tools, namely Cadence Virtuoso. If that is not the case please follow the link below and follow steps 1, 2, and 3 of the "Environment & Tool Setup" section.

http://icslwebs.ee.ucla.edu/dejan/classwiki/index.php/Tool_Setup

Note: Please make sure to comment the following line (use the # character) before sourcing the *tool-setup* file.

```
source /w/apps3/Synopsys/Liberty_NCX/vG-2012.06/SETUP
```

Copy Model Library Path

In order to follow this tutorial you will need to copy the technology model library into your *ee216a* directory. You can do this by executing the following line from within your *ee216a* directory.

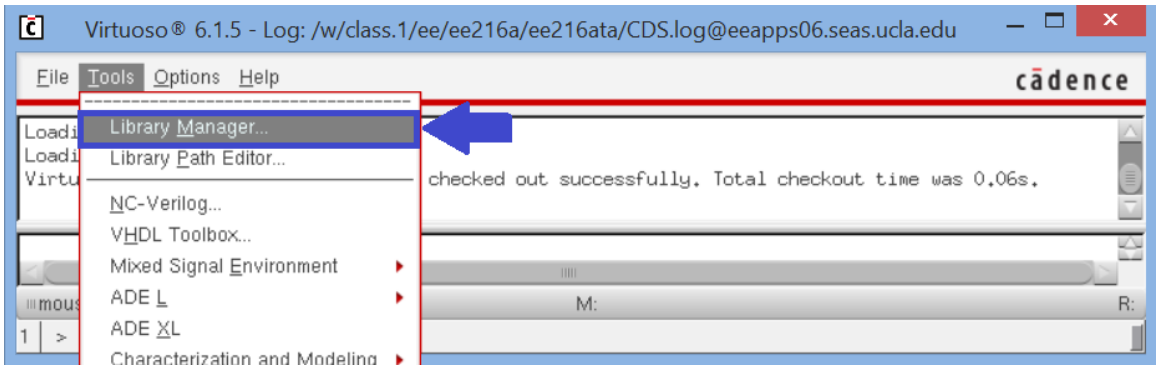
```
cp /w/class.1/ee/ee216o/ee216ota/setup/saed32nm.lib .
```

NMOS and PMOS Device Simulation in Virtuoso 6.1.4

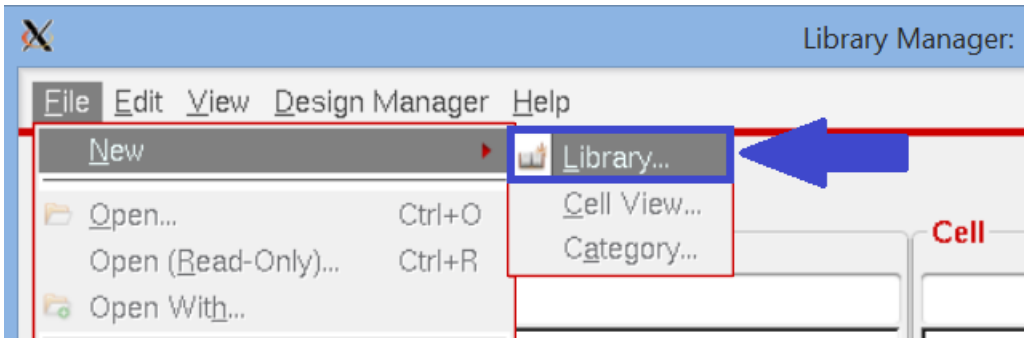
- **Run Virtuoso** from within ee216a directory

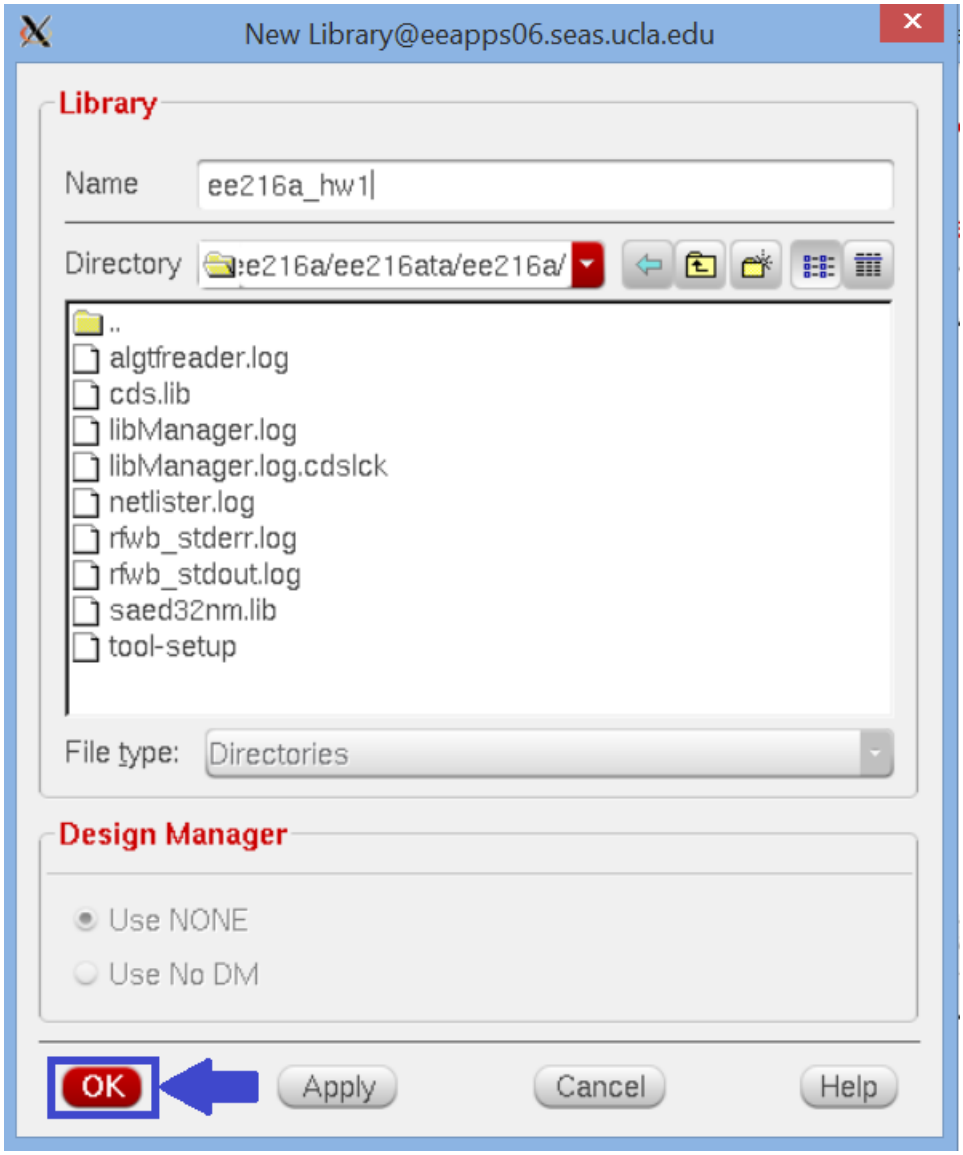
```
[ee216ata@eeapps06 ~]$
[ee216ata@eeapps06 ~]$ cd ~/ee216a
[ee216ata@eeapps06 ~/ee216a]$ source tool-setup
[ee216ata@eeapps06 ~/ee216a]$ virtuoso &
```

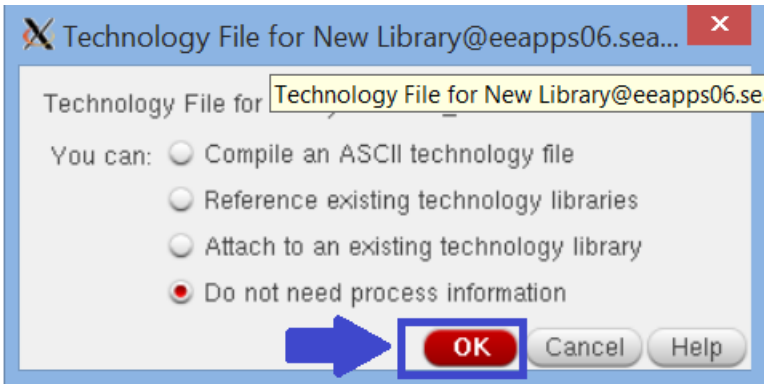
- **Open "Library Manager"** – Tools -> Library Manger



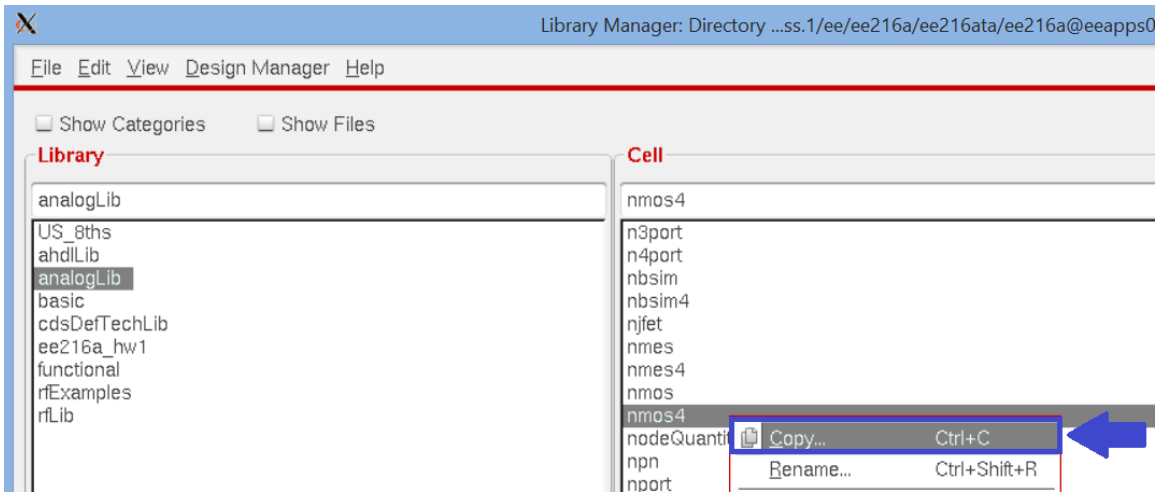
- **Create a new library** named "ee216a_hw1" – File -> New -> Library

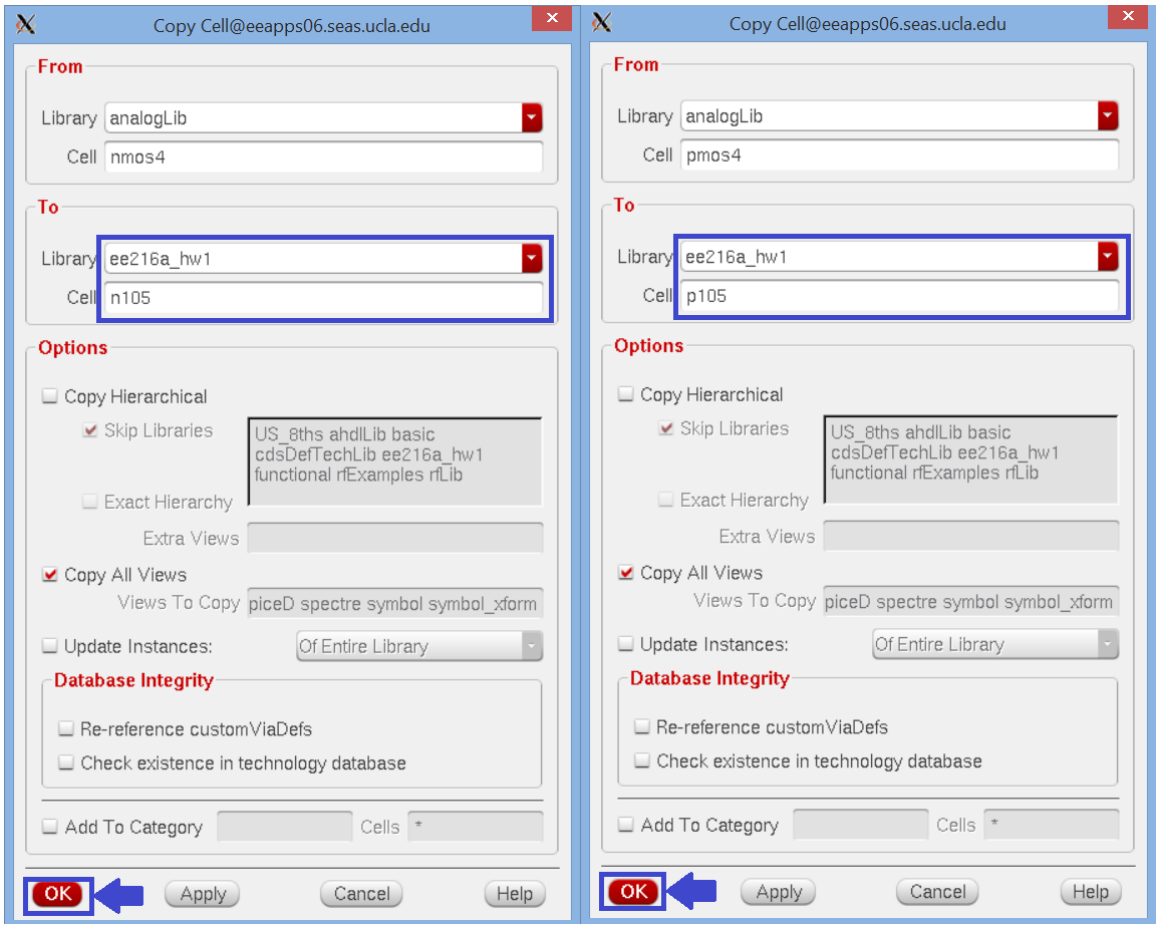



New Library@eeapps06.seas.ucla.edu
Library
Name
ee216a_hw1
Directory
:e216a/ee216ata/ee216a/
..
algtfreader.log
cds.lib
libManager.log
libManager.log.cdslck
netlister.log
rfwb_stderr.log
rfwb_stdout.log
saed32nm.lib
tool-setup
File type:
Directories
Design Manager
Use NONE
Use No DM
OK
Apply
Cancel
Help

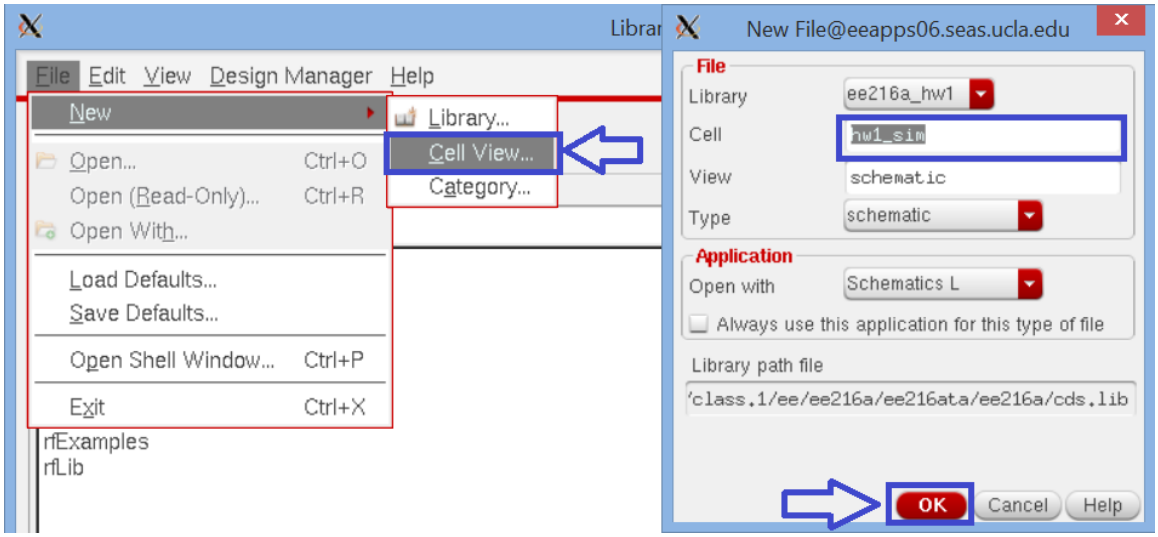

Technology File for New Library@eeapps06.sea...
Technology File for
Technology File for New Library@eeapps06.se
You can:
Compile an ASCII technology file
Reference existing technology libraries
Attach to an existing technology library
Do not need process information
OK
Cancel
Help

- **Copy the nmos4 and pmos4 devices from *analogLib* library to newly created *ee216a_hw1* library as n105 and p105 respectively** – right-click on nmos4 and pmos4 and click copy





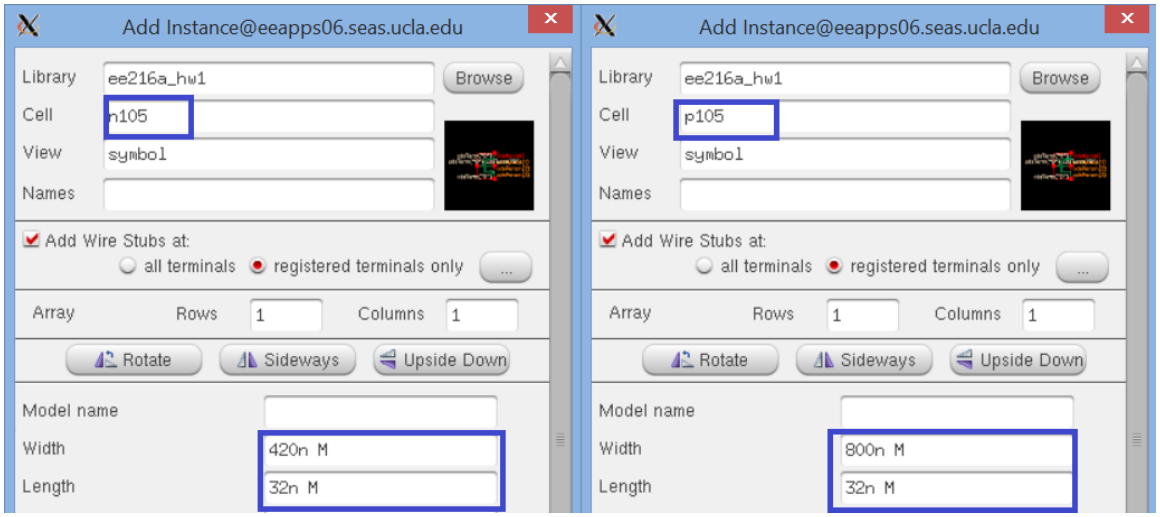
- **Create a new Cell-view for a schematic**

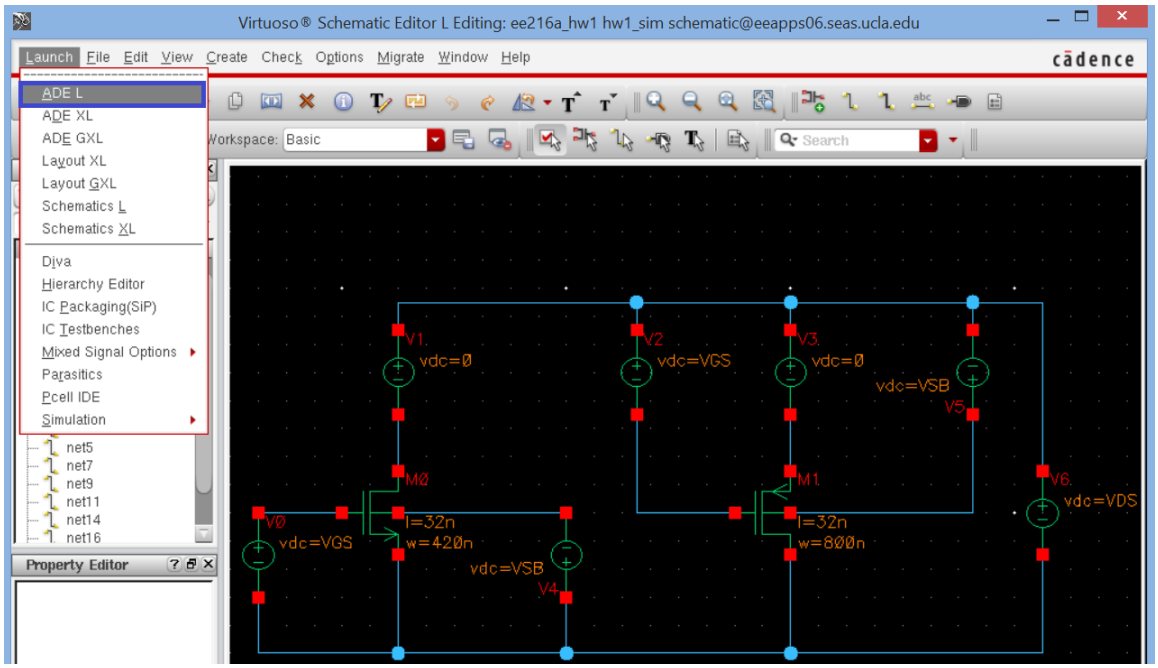


- **Create the following schematic using n105 and p105 for the NMOS and PMOS respectively**. When instantiating n105 and p105 use the following widths and lengths -

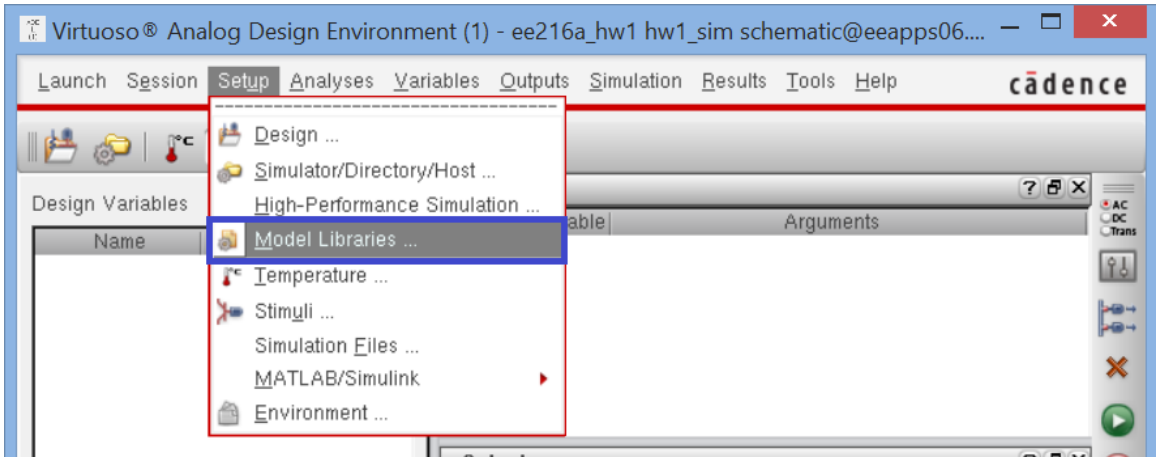
(W/L)n = 420nm/32nm, (W/L)p = 800nm/32nm.

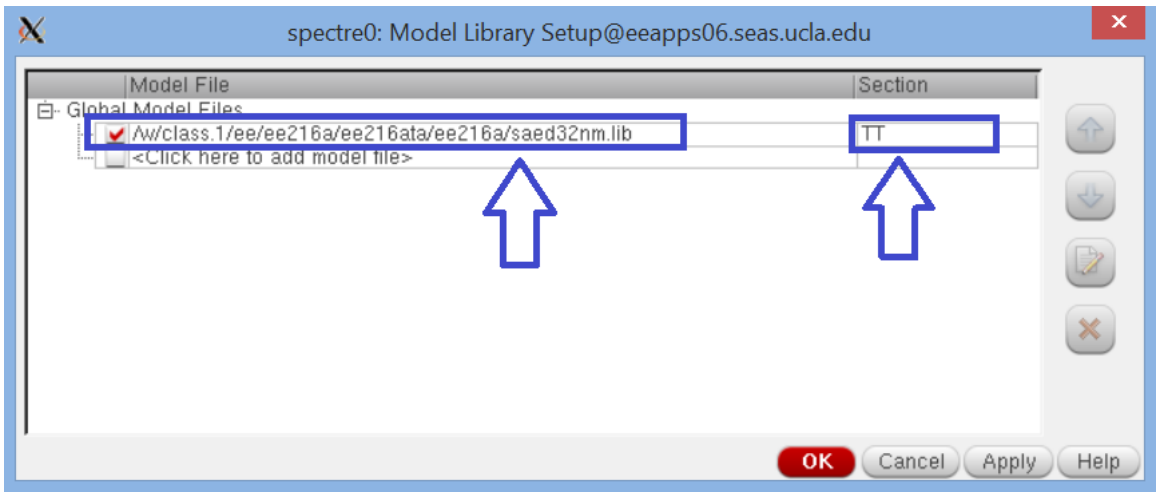
The n105 and p105 devices in the 32nm library are modeled by a sub-circuit. To avoid issues with saving and plotting the current through the ports of sub-circuits place a 0V dc voltage source in series with whatever port you are trying the measure the current of (i.e. the drains of the NMOS and PMOS). And measure the current through the voltage source instead.



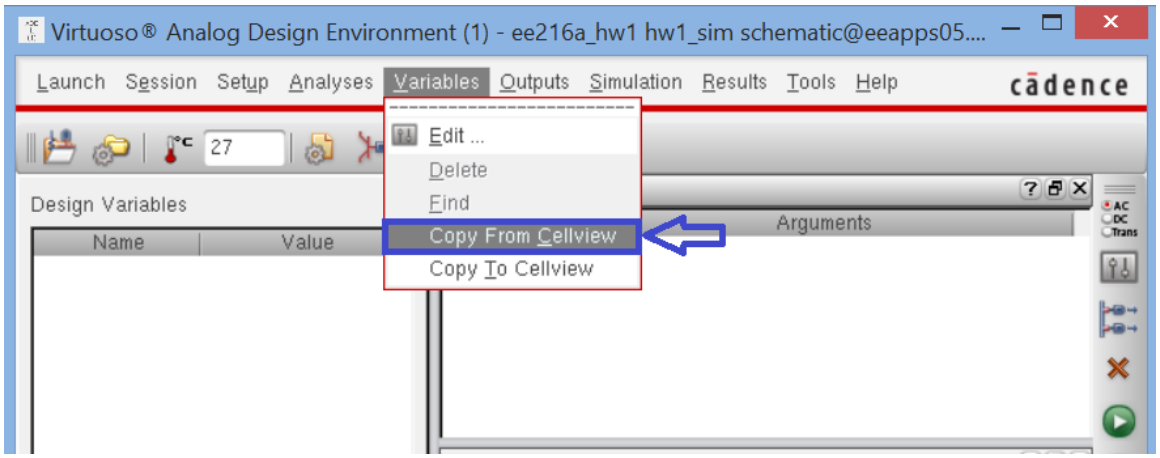


- **Specify saed32nm.lib as the simulation model library with "TT" corner** – Setup -> Model Libraries.

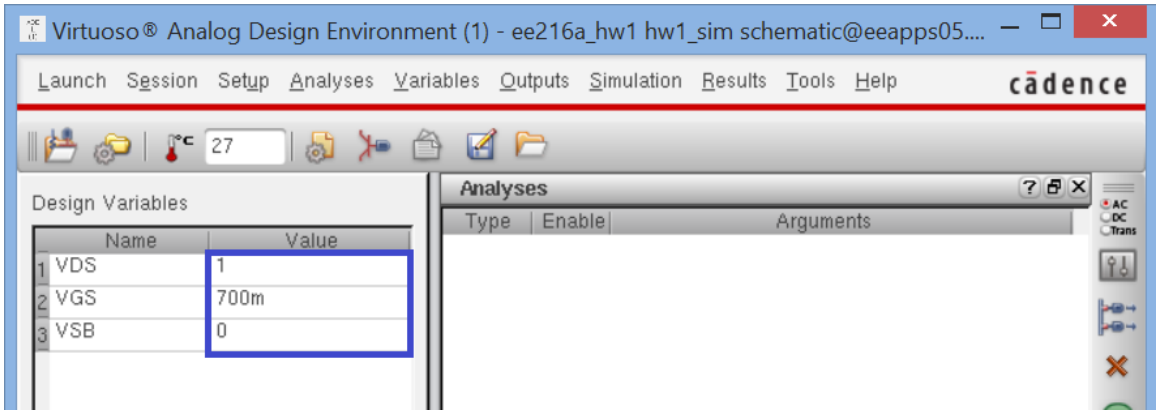




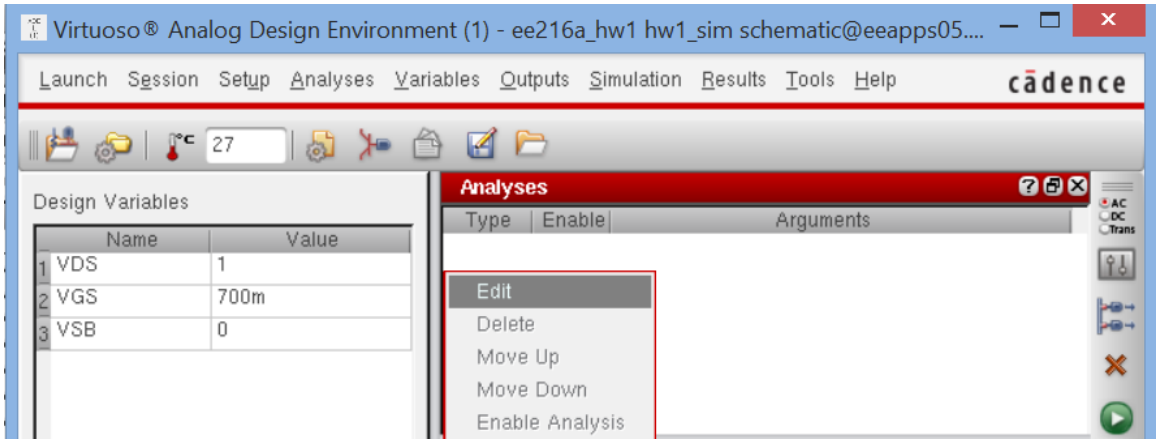
- **Import the variables from the schematics** – Variables -> Copy From Cellview

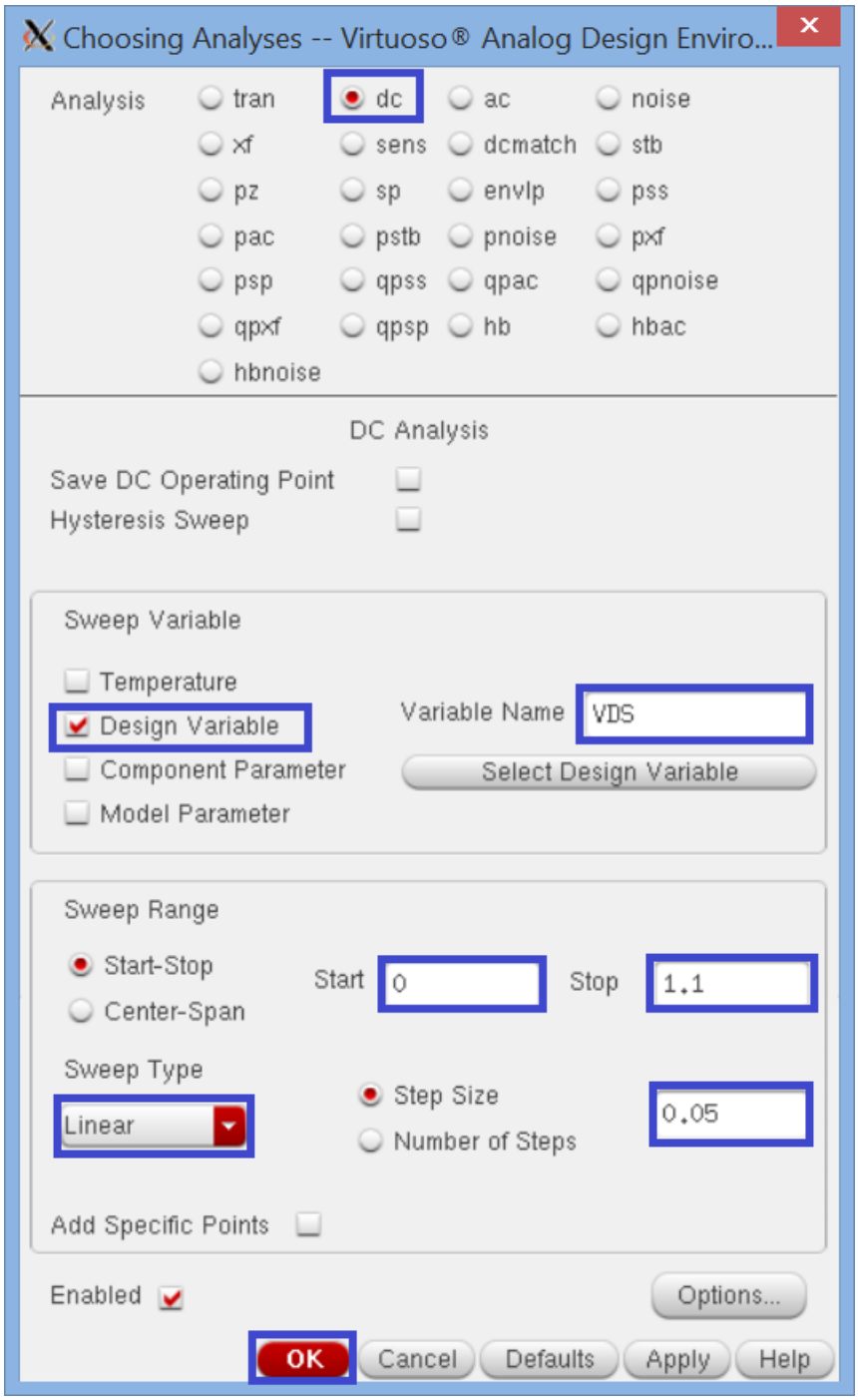


- **Set the default variable values** – i.e. VDS = 1V, VGS = 700mV, VSB = 0V

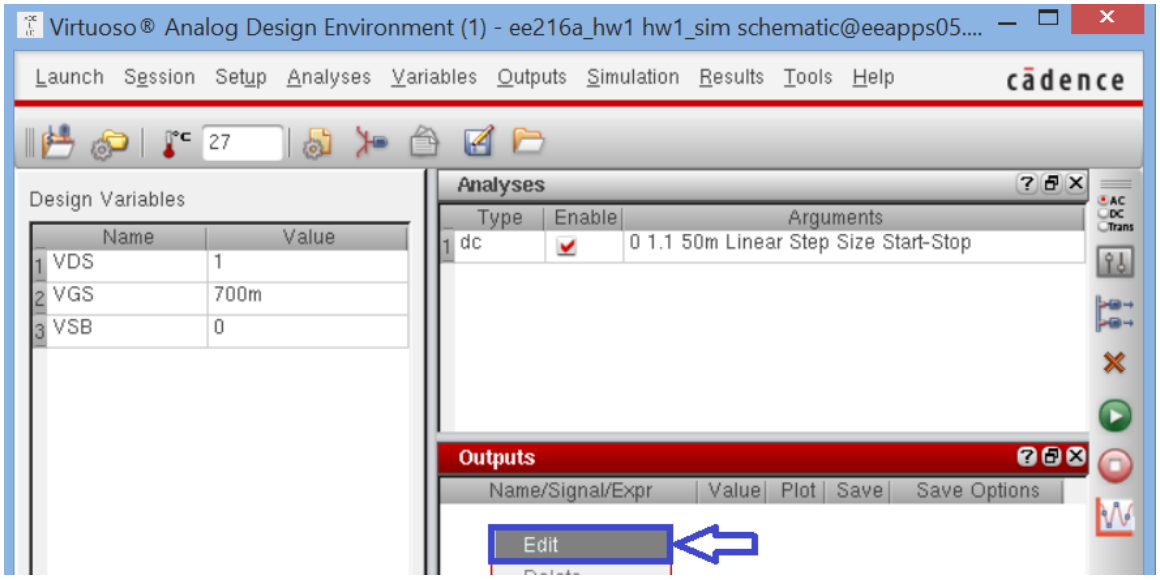


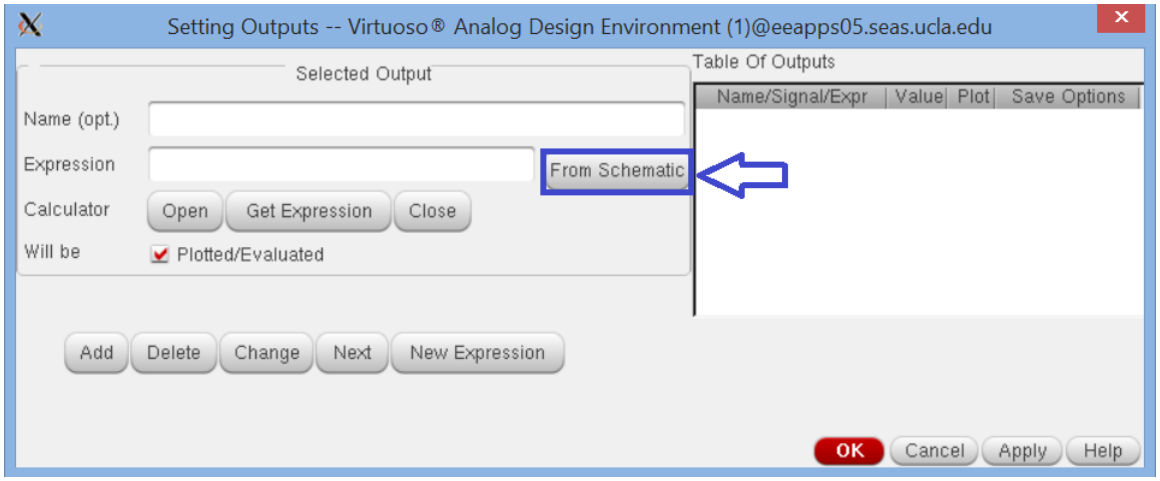
- **Select type of simulation you want to run** – right-click in the Analysys pane and click edit. In this example we will run a DC sweep for the VDS from 0 to 1.1V in 50mV steps

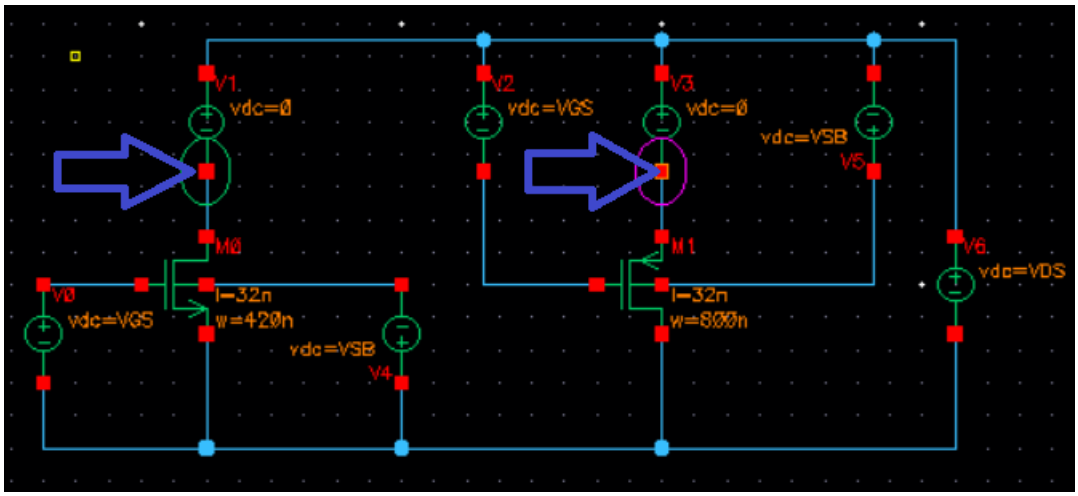


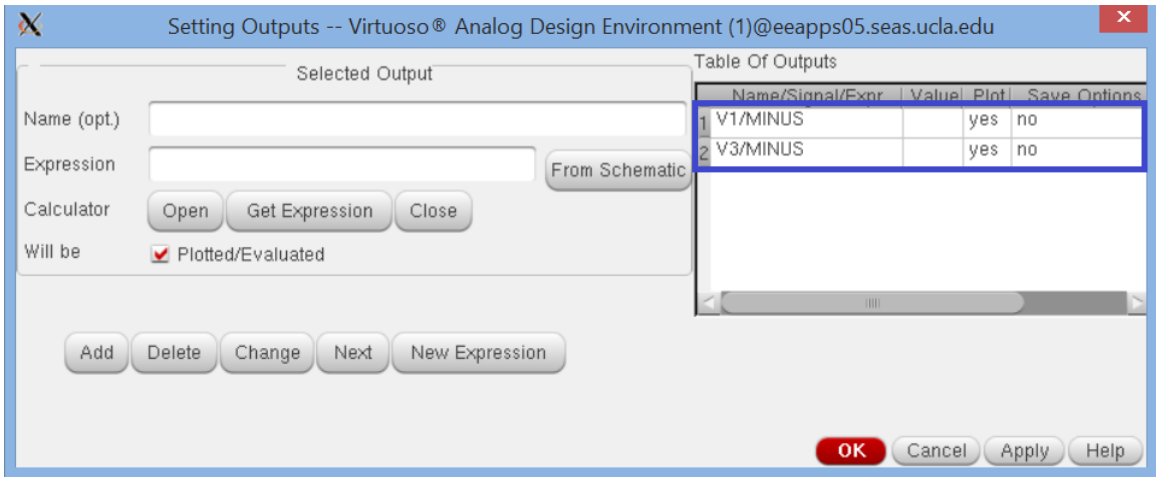


- **Next, select the outputs you would like to observe** – right-click in the "Outputs" pane and select "Edit", click "From Schematic" button and select the V1 and V3 terminals (circles will appear). If you now go back to the "Outputs" pane you will see these terminals in the "Table of Outputs" pane.

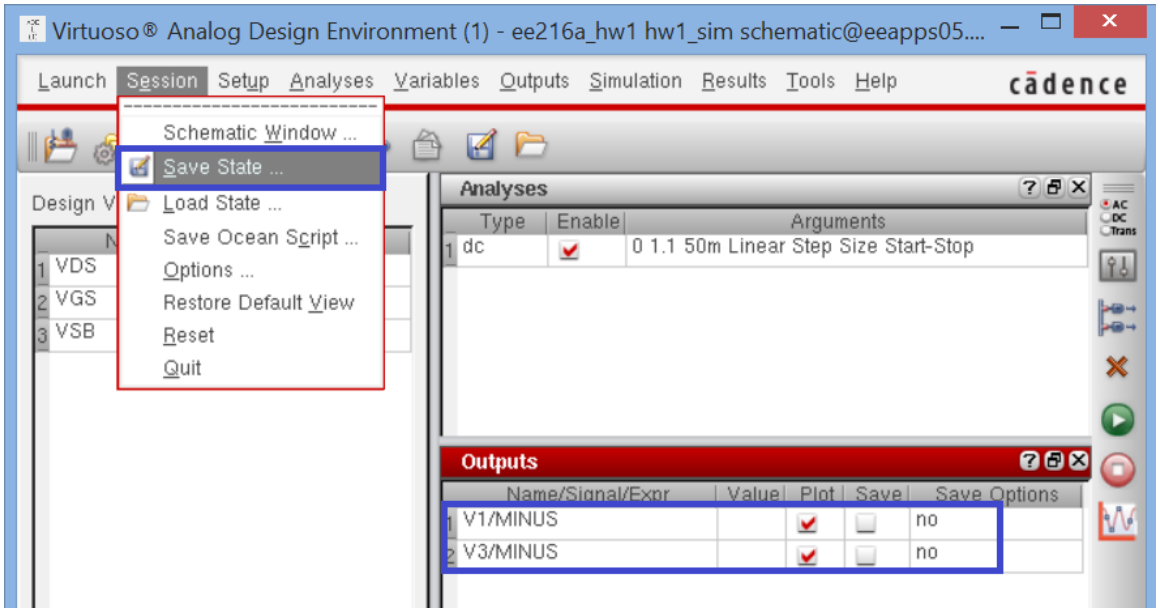

Virtuoso® Analog Design Environment (1) - ee216a_hw1 hw1_sim schematic@eeapps05....
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help
cadence
27
Design Variables
Name Value
1 VDS 1
2 VGS 700m
3 VSB 0
Analyses
Type Enable Arguments
1 dc 0 1.1 50m Linear Step Size Start-Stop
Outputs
Name/Signal/Expr Value Plot Save Save Options
Edit

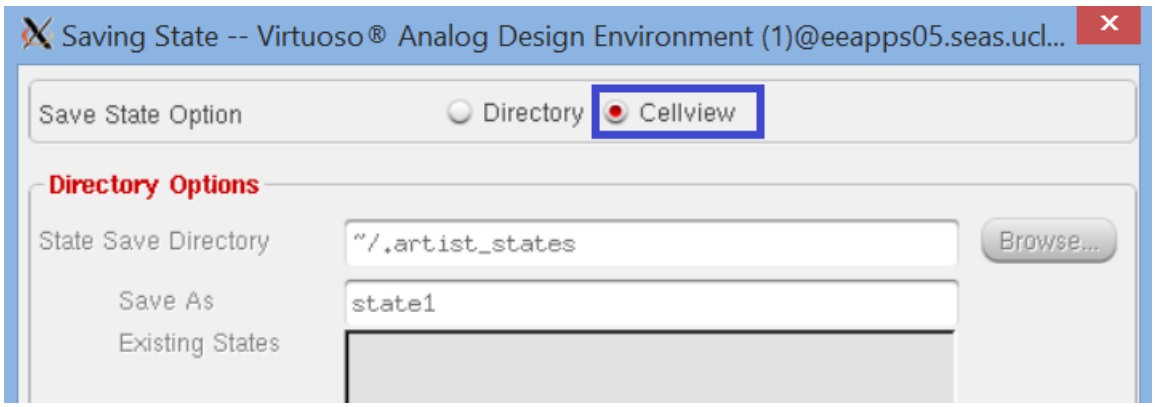

Setting Outputs -- Virtuoso® Analog Design Environment (1)@eeapps05.seas.ucla.edu
Selected Output
Name (opt.)
Expression
From Schematic
Calculator
Open
Get Expression
Close
Will be
Plotted/Evaluated
Table Of Outputs
Name/Signal/Expr Value Plot Save Options
Add
Delete
Change
Next
New Expression
OK
Cancel
Apply
Help


V1
vdc=0
V2
vdc=VGS
V3
vdc=0
vdc=VSB
V5
M0
M1
V0
vdc=VGS
l=32n
w=420n
w=800n
vdc=VSB
V4
V6
vdc=VDS



- **Save the state in Cellview** – Session -> Save State -> Cellview





- **Run the simulation and observe the selected outputs.**