ECE 216B VLSI Signal Processing **Spring 2024**

Prof. Dejan Marković Homework #1

Solution

Problem 1. Delay Model

a) Typical corner: $\mathbf{K_d = 13.92}$, $\mathbf{V_{on} = 0.22}$, $\mathbf{\alpha_d = 2.16}$

b) V_{DD}@minEDP = **0.7V** (**typical and slow**), **0.5V** for **fast** corner

c) Worst-case delay is in the **slow corner**. The delay ratio (from the provided simulation data) is 99ps/36ps. Therefore, $f_{clk}(1V)$ = 99/36*250 MHz = **687.5 MHz**.

Problem 2. Research Paper Study

Answers may vary (open-ended question).

Problem 3: Inverter Chain Optimization

a) Using Excel solver or analytically (partial derivatives): $\boldsymbol{x_2 = 2.83}$, $\boldsymbol{x_4 = 8}$, $\mathbf{D_{min} = 11.66}$.

b) Energy at stage k is proportional to the total output capacitance of stage k, $C_{out,k} = (\gamma * C_k + C_{k+1})$. Sum energy of all four stages and include the switching activity, $\mathbf{E_{tot} = 4.275}$.

c) Using Excel solver: $\boldsymbol{x_2 = 2.15}$, $\boldsymbol{x_4 = 4.06}$, $\mathbf{E(1.1D_{min}) = 3.582}$ **(a 16% reduction)**.