Lecture

13

ECE 216B

SDR Architecture Optimization

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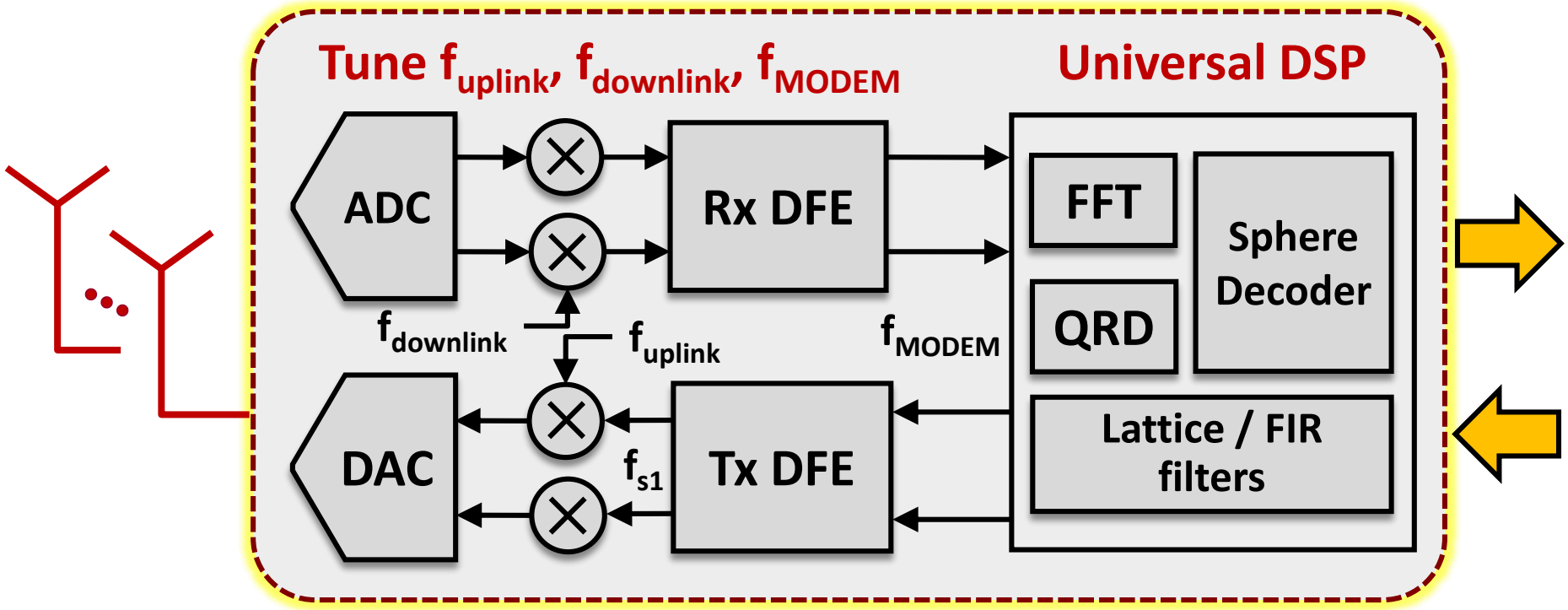
Lecture material based on PhD project of Rashmi Nanda (now at Qualcomm)

Motivation

- **Flexible radios**
  - Large # of frequency bands
  - Integrate GPS and WLAN
  - Demands high complexity, low power
- **New wide-band standards**
  - Long term evolution (LTE) cellular – 0.7 GHz to 2.7 GHz
  - WiMAX – 2.3 GHz to 2.7 GHz
- **Digital front ends (DFE)**
  - DSP techniques for high flexibility with low power

Towards Cognitive Radio

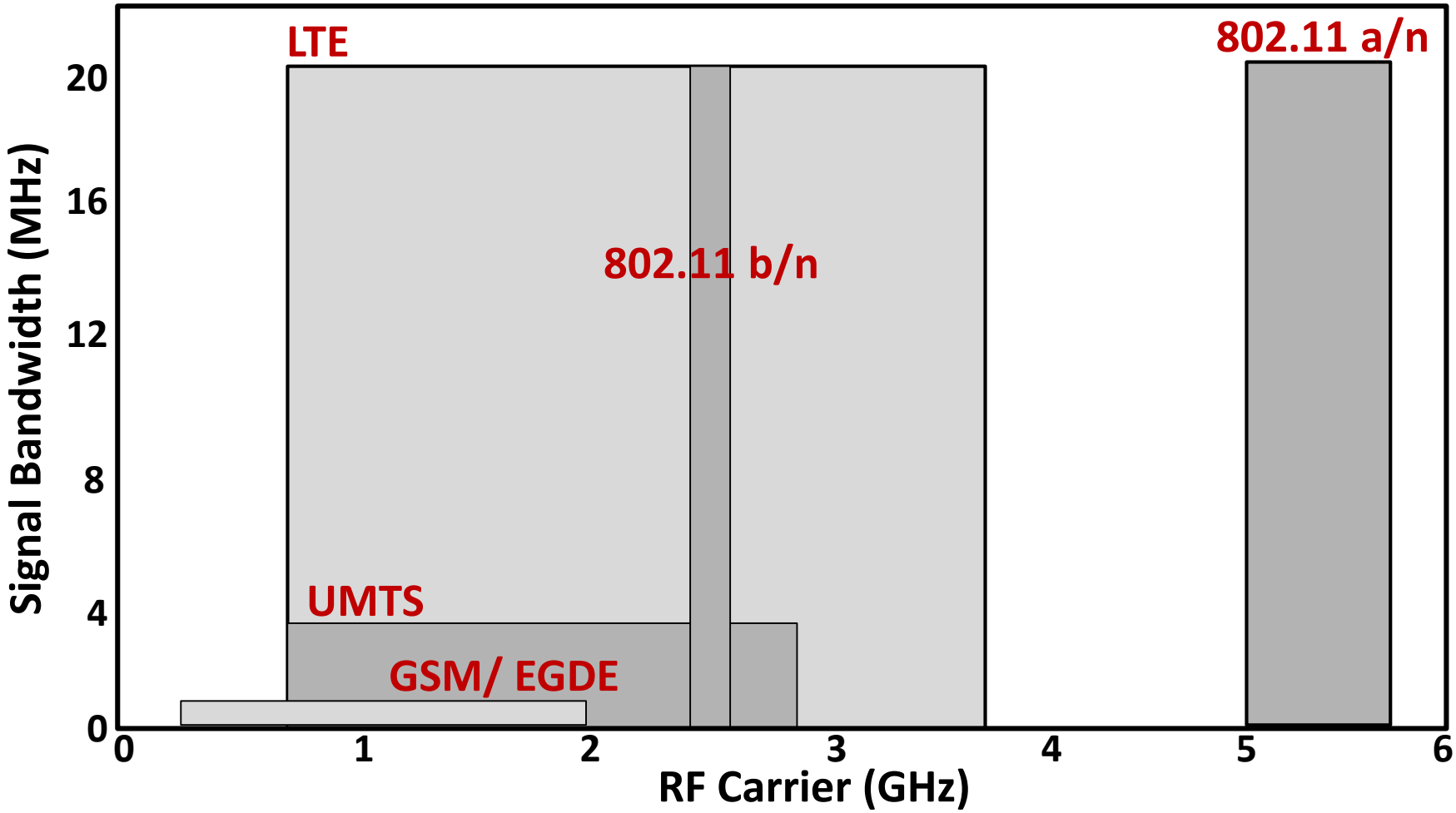
On-the-fly tuning: RF carrier, signal BW, DSP algorithms



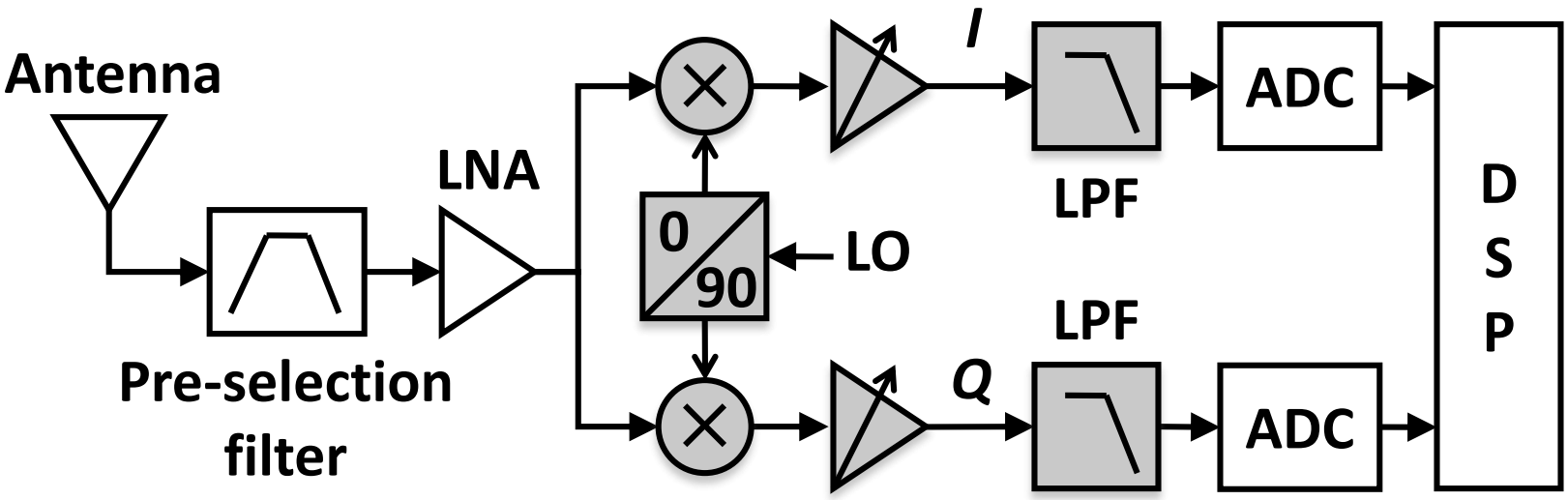
Flexibility with min. area & power penalty?

Reconfigurable Frequency Bands

- Wide range of RF carrier frequencies
- Support for multiple data bandwidths

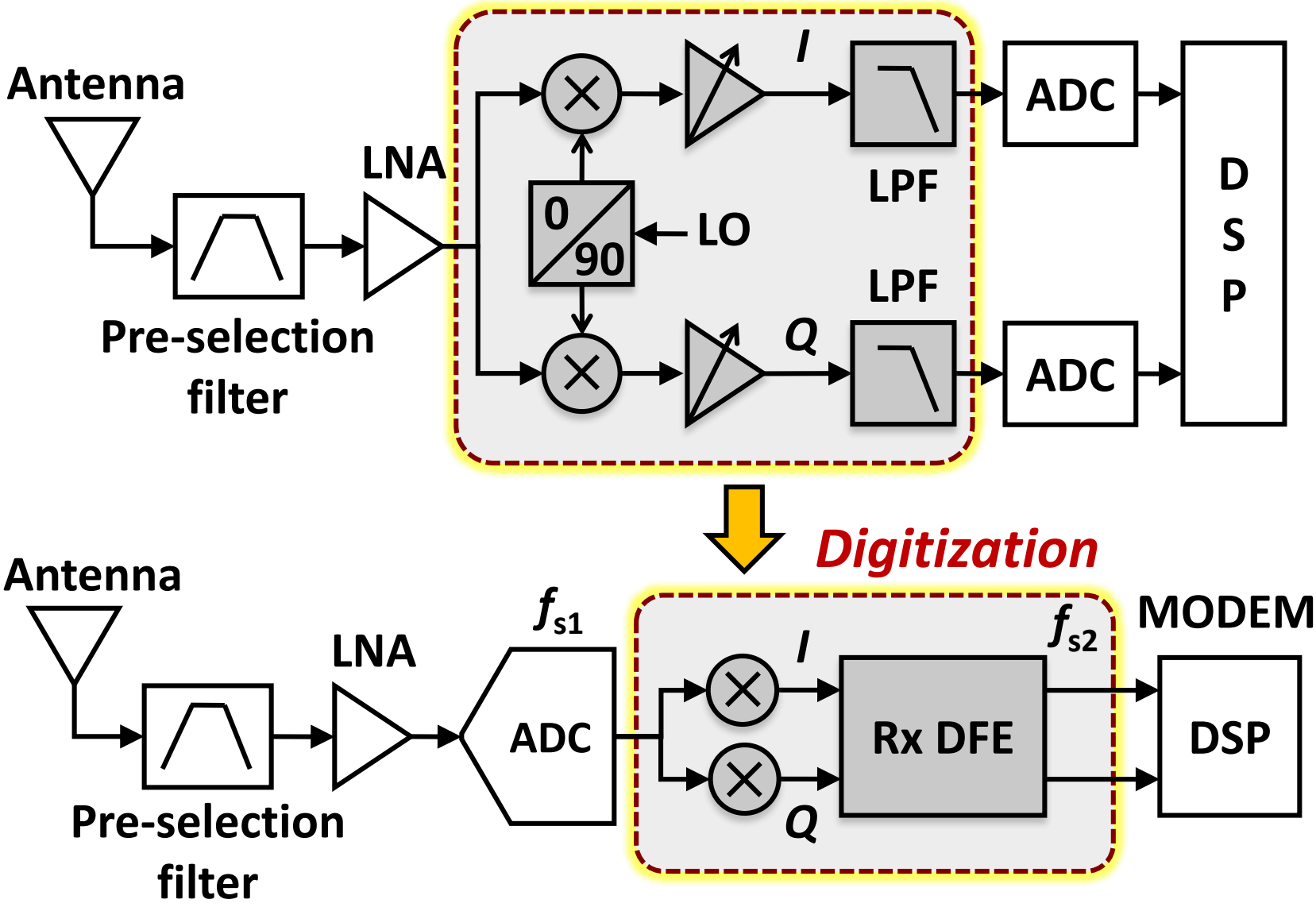


Conventional Rx Architecture



- **Variable f_{RF}, BW for multi-standard support**
  - Difficult to incorporate tuning knobs in analog
  - RF filters are bulky and costly
- **Non-scaling of analog power**

Digitizing Rx Front-End (RxDFE)



DFE: Benefits and Challenges

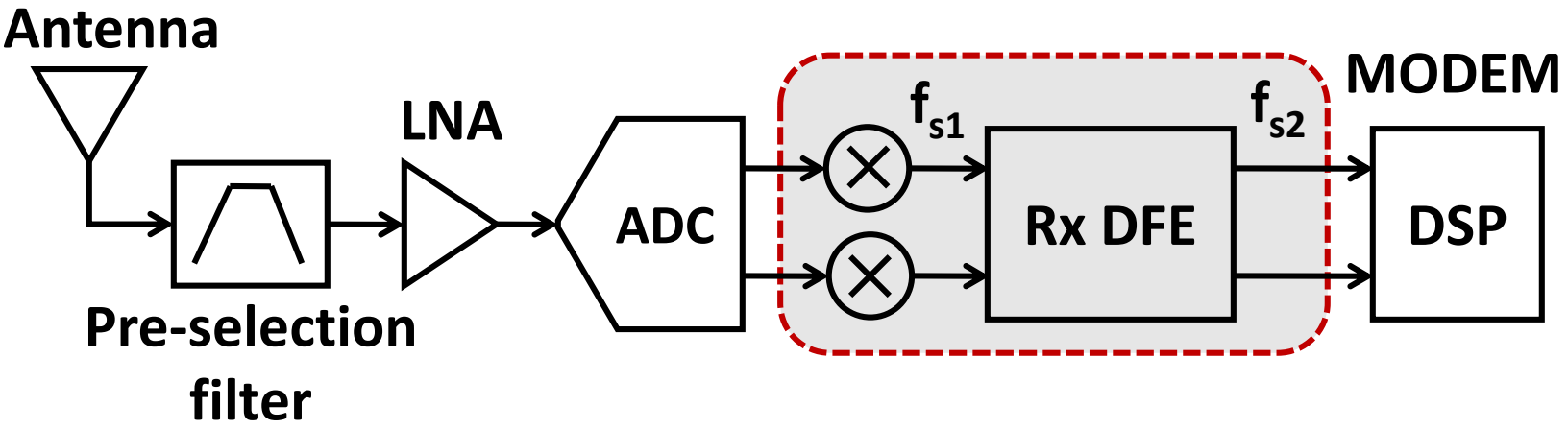
- **Benefits:**
  - Easy programmability
  - Small area and low power of the DSP components
- **Challenges:**
  - More complex ADC, which has to work at GHz speeds [1]
  - Some DSP blocks have to process GHz-rate signals
- **Some existing solutions:**
  - Intermediate-frequency ADC, analog filtering and digitization [2]
  - Discrete-time signal processing for signal conditioning [3]

[1] N. Beilleau *et al.*, "A 1.3V 26mW 3.2GS/s Undersampled LC Bandpass ΣΔ ADC for a SDR ISM-band Receiver in 130nm CMOS," in *Proc. Radio Frequency Integrated Circuits Symp.,* June 2009, pp. 383-386.

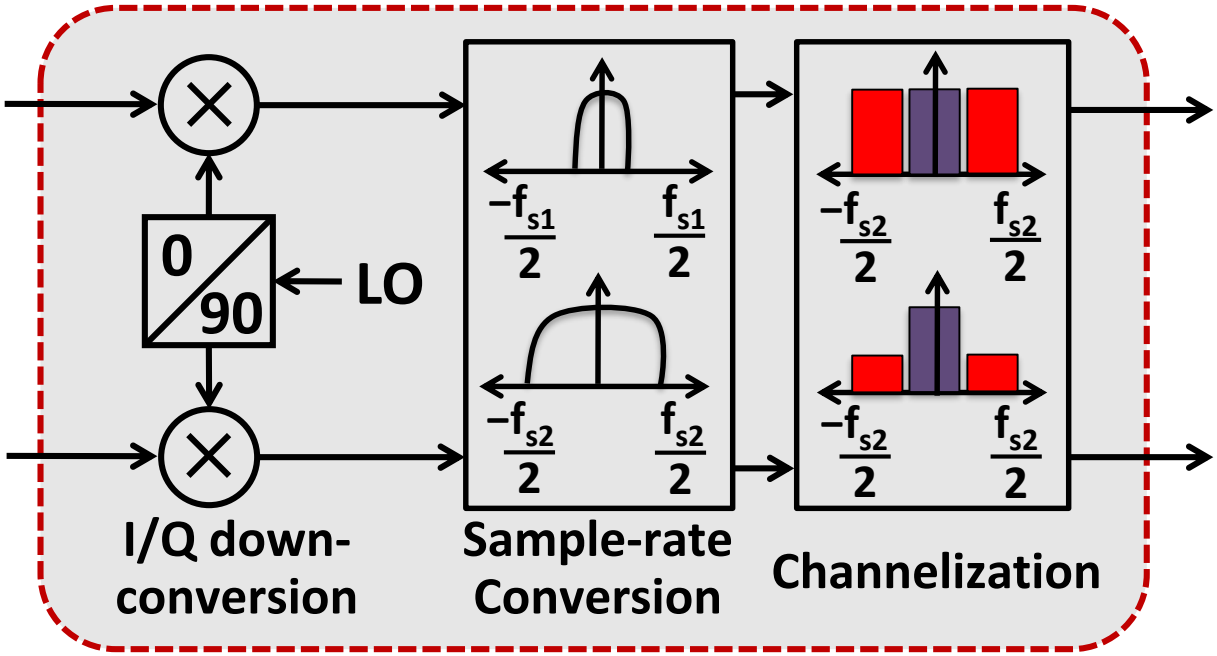
[2] G. Hueber *et al.*, "An Adaptive Multi- Mode RF Front-End for Cellular Terminals, " in *Proc. Radio Frequency Integrated Circuits RFIC Symp.,* June 2008, pp. 25-28.

[3] R. Bagheri *et al.,* "An 800MHz to 5GHz Software-Defined Radio Receiver in 90nm CMOS," in *Proc. Int. Solid-State Circuits Conf.,* Feb. 2006, pp. 480-481.

Rx DFE Functionality

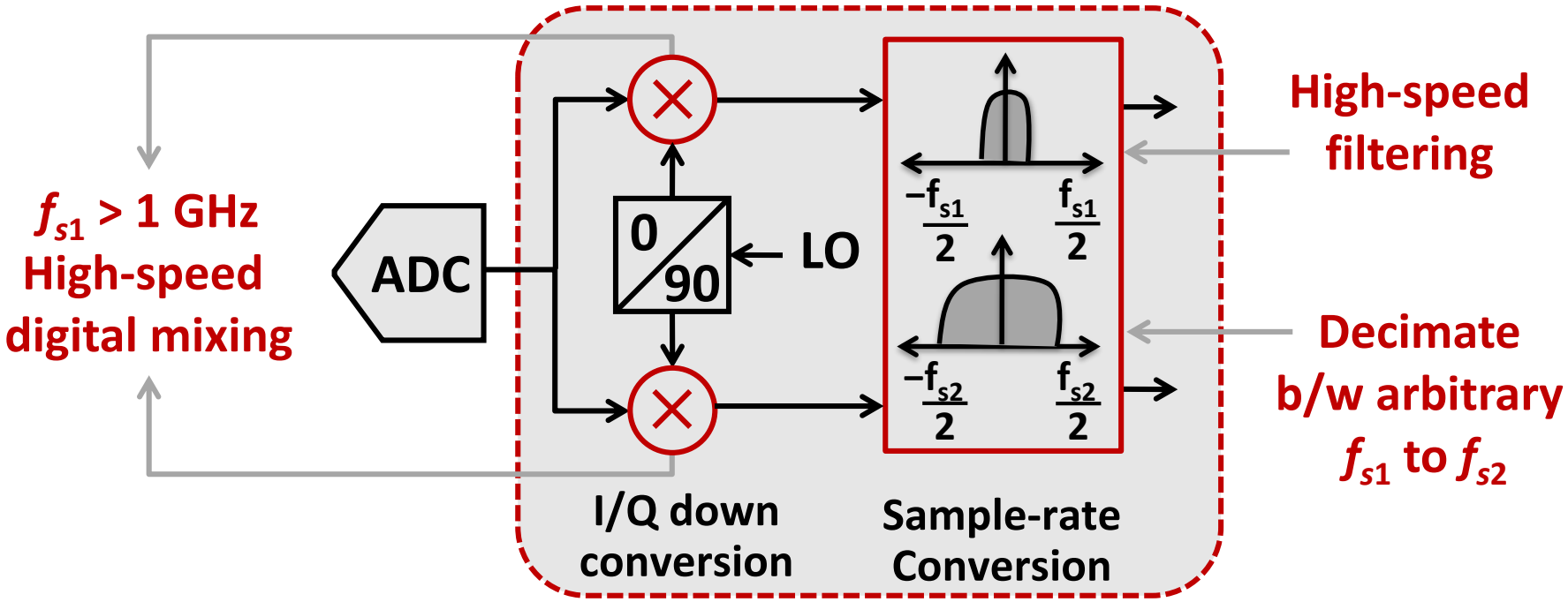


Convert from ADC frequency f_{s1} to modem frequency f_{s2} with negligible SNR degradation

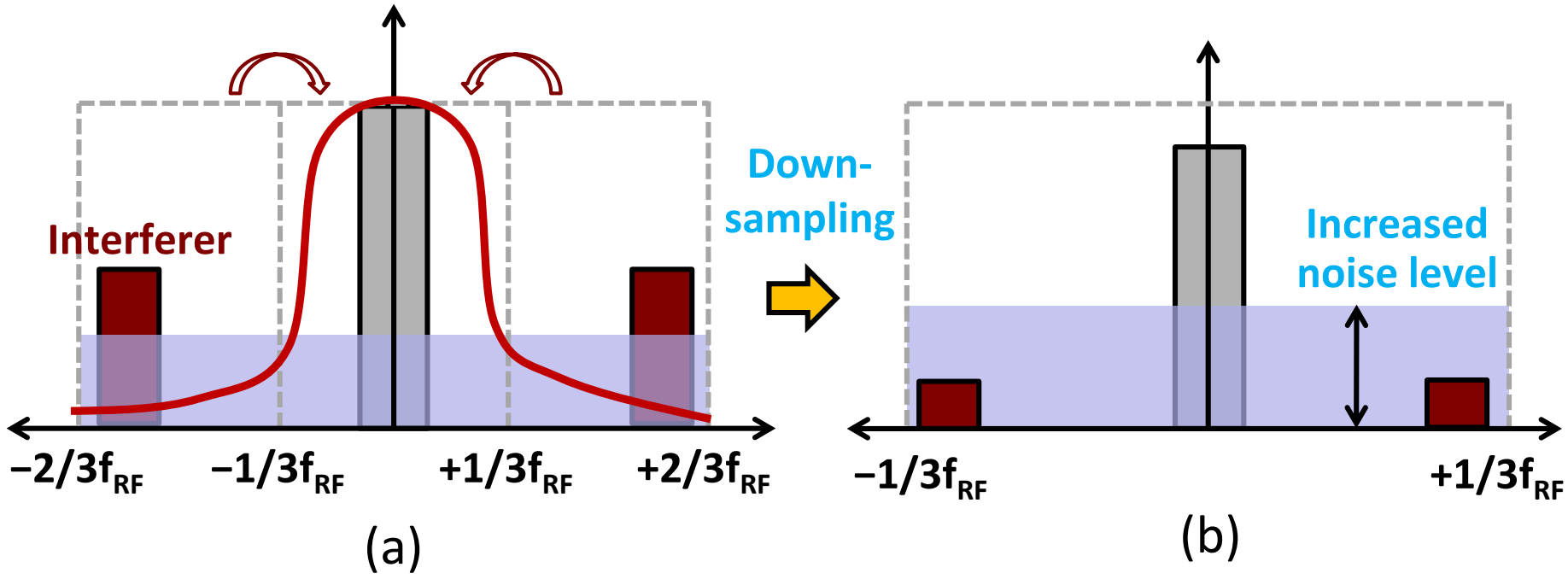


Challenge #1: Down-Conversion & Decimation

- **Rx DFE Design**
  - Carrier multiplication (digital mixing) at GHz frequencies
  - Anti-aliasing filters next to the ADC function at GHz rate
  - Architecture must support fractional decimation factors
  - Low power requirement for mobile handset applications



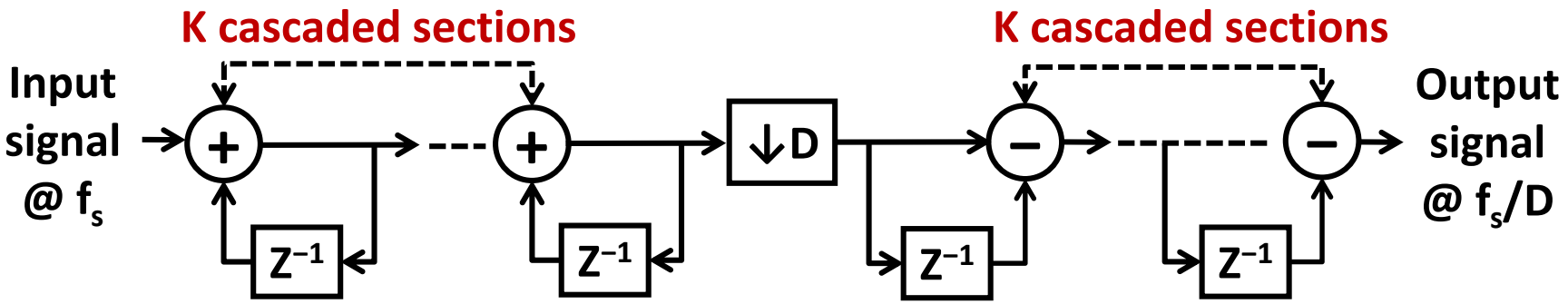
Rx DFE Sample-Rate Conversion



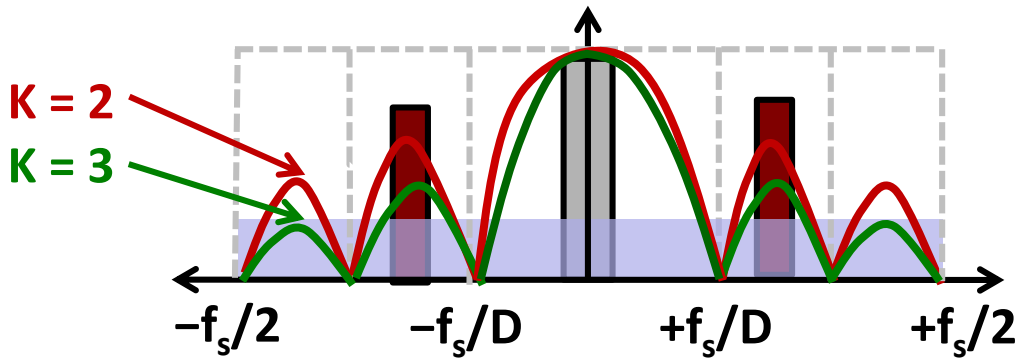
- **Sources of noise during sample-rate conversion**
  - Out-of-band noise aliases into desired frequency band
  - DFE must suppress noise
  - SNR degradation limited to 2-3 dB

Cascaded CIC Decimation Filters

- **Generalized CIC filters**
  - K cascaded section of integrators and differentiators
  - K > 1 required for higher out of band attenuation
  - Adjacent sections can be pipelined to reduce critical path

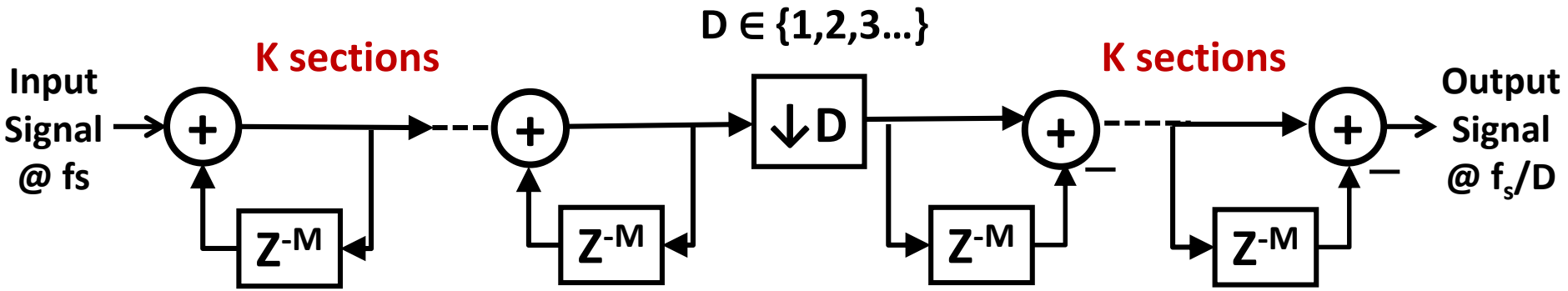


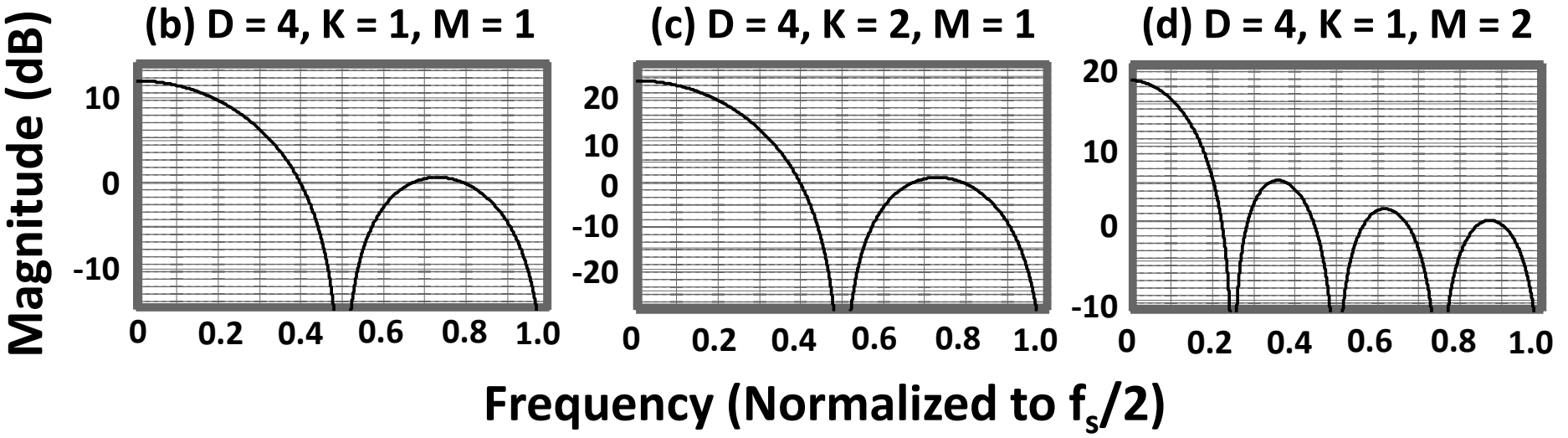
$$\frac{(1-z^{-D})^K}{(1-z^{-1})^K}$$



Reconfigurable CICs

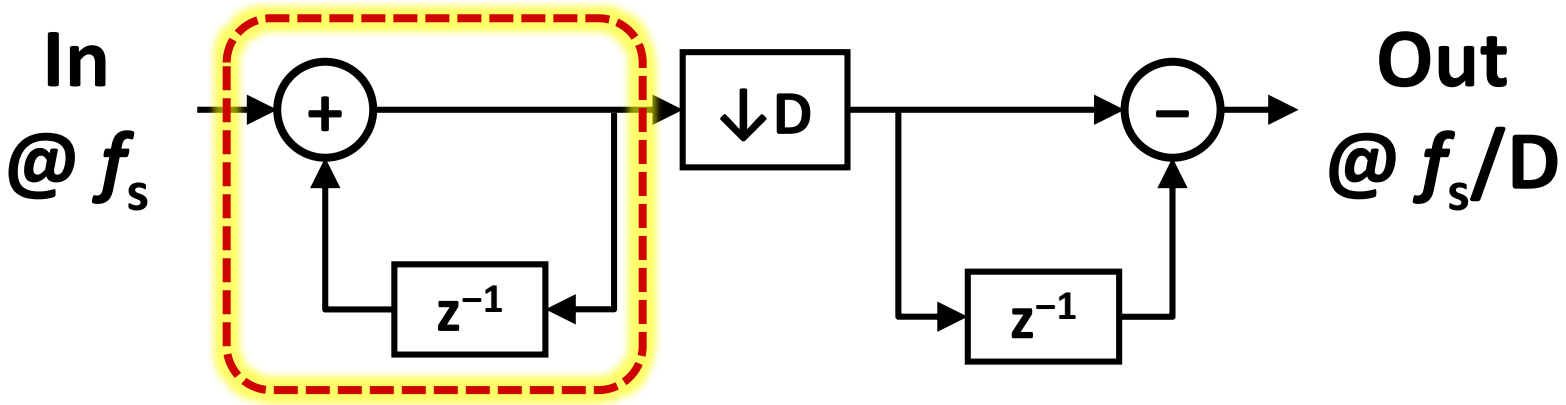
- Control frequency response using parameters D, M, K
- Suitable for programmable filters





CIC Decimation Filters

Recursive, long wordlength, throughput limited

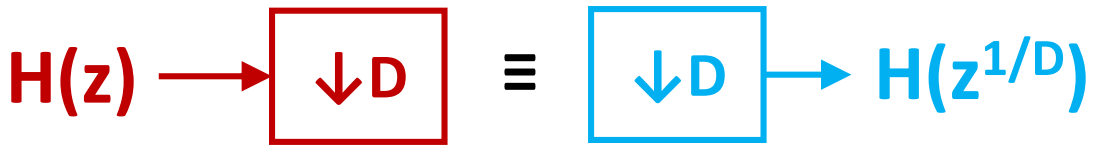


Throughput Limited

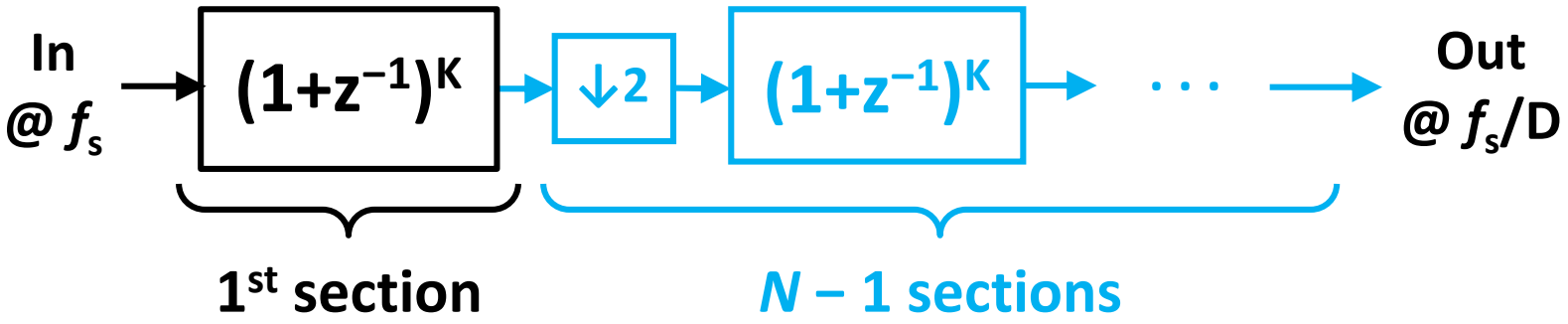
Feed-forward CIC Structure

$$\frac{(1-z^{-D})^K}{(1-z^{-1})^K} = (1+z^{-1})^K\,(1+z^{-2})^K \ldots (1+z^{-2^{N-1}})^K$$

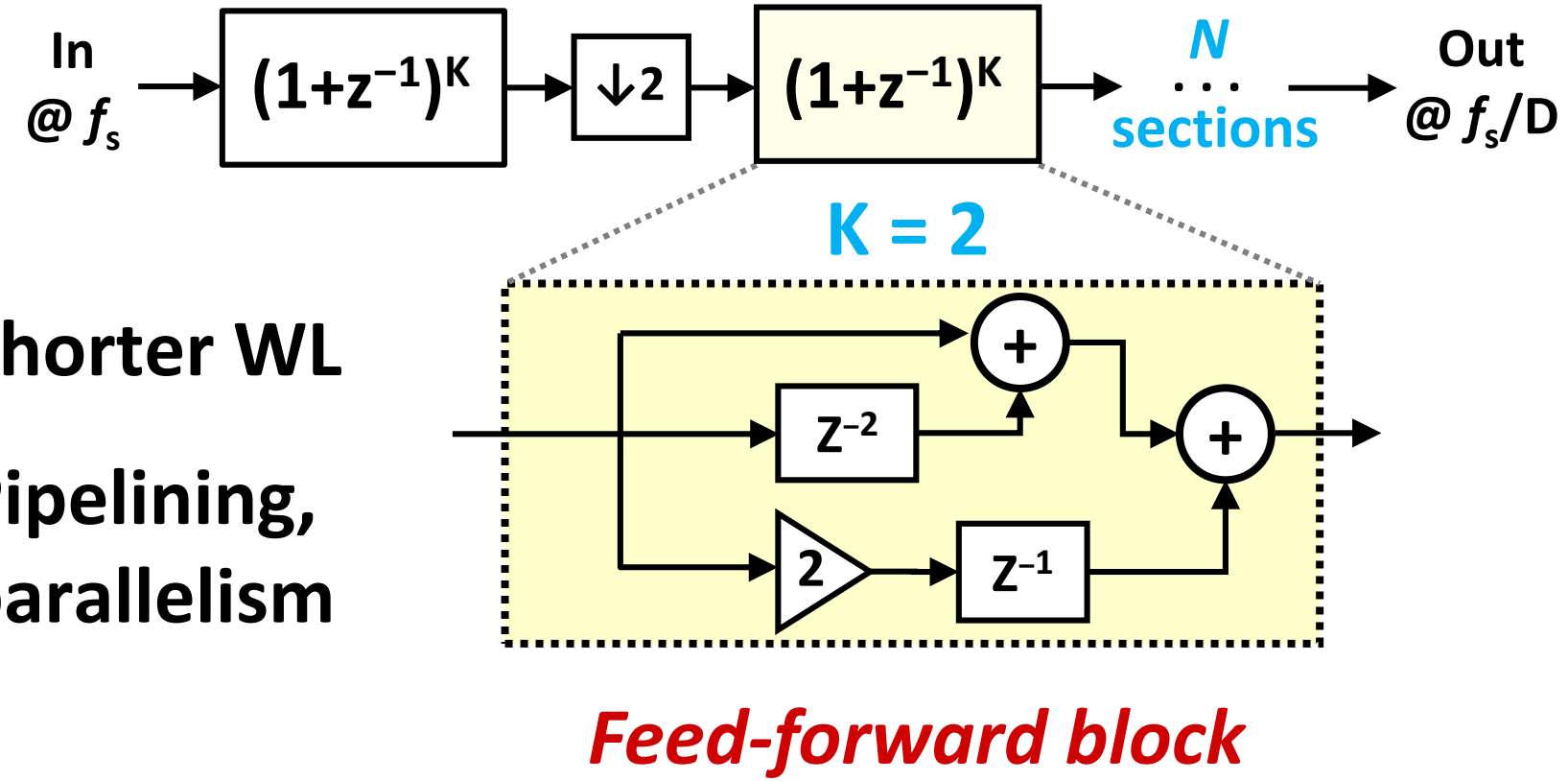
$N = \log_2(D)$



Cascaded realization



Cascaded CIC Architecture

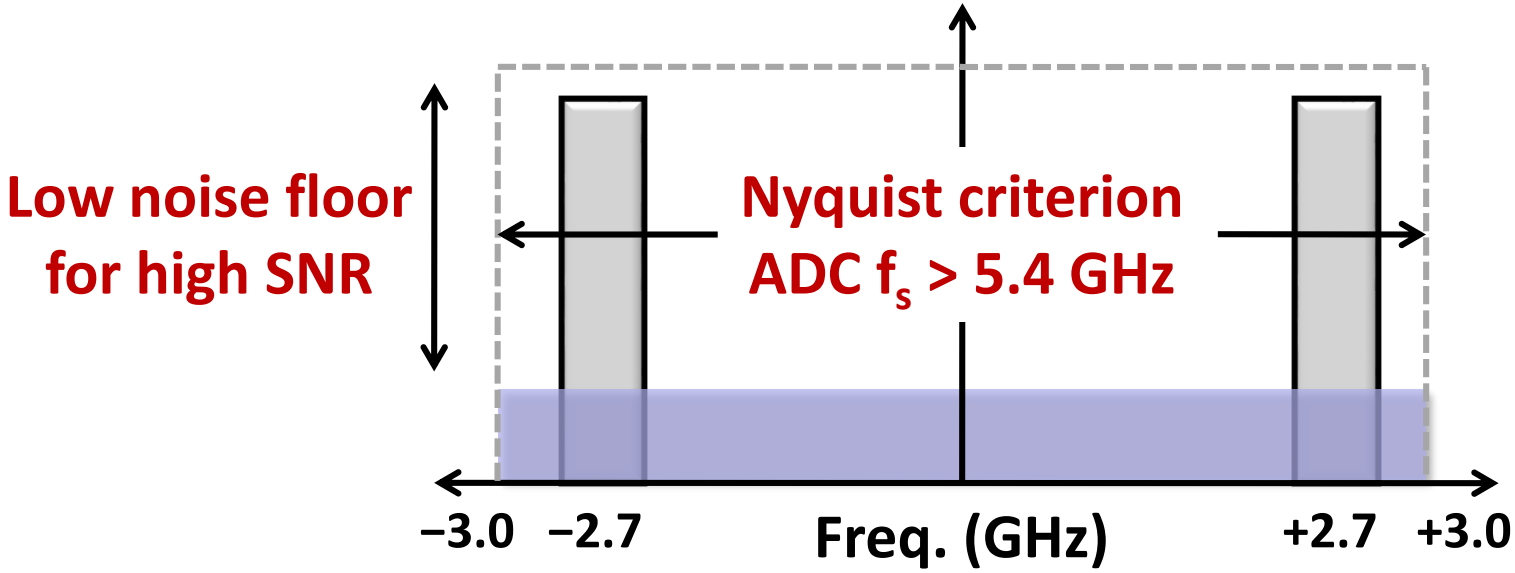


- Shorter WL
- Pipelining, parallelism

Feed-forward block

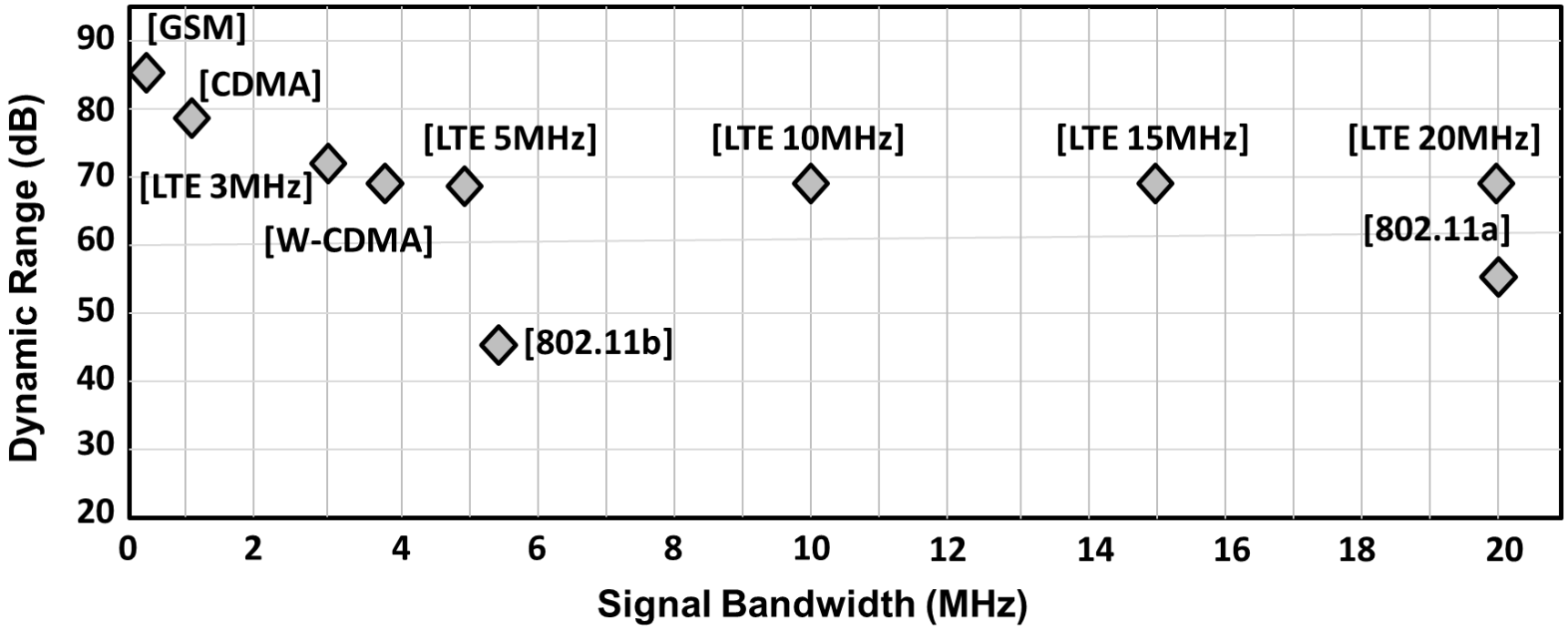
Rx DFE Challenge #1: Very High-Speed ADC

- Nyquist criterion demands $f_s > 2f_{RF}$
- For RF carrier beyond 1 GHz, f_s very high
- Digitizing the RF signal needs large ADC bandwidth
- High dynamic range for wide-band digitization



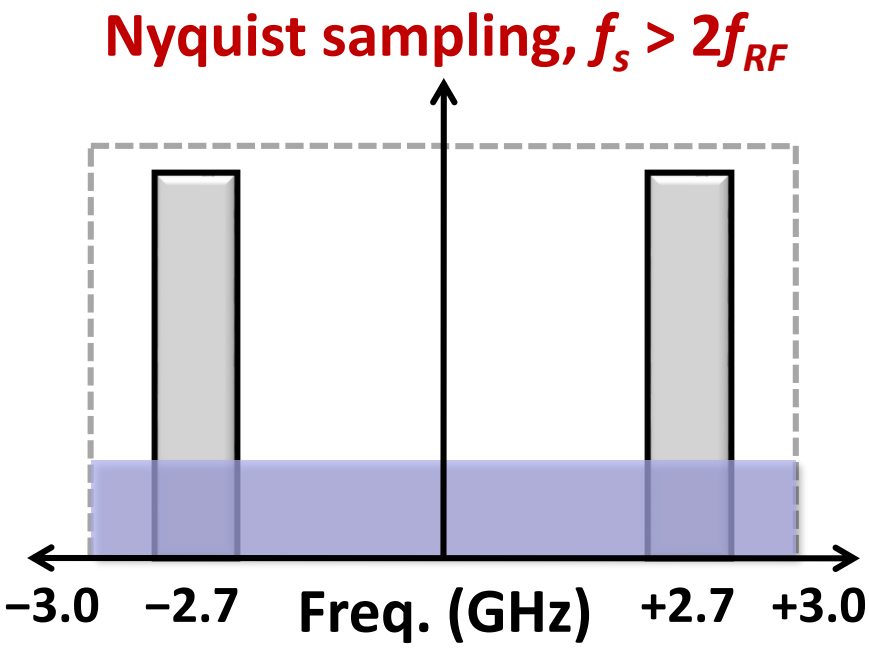
Rx Dynamic Range

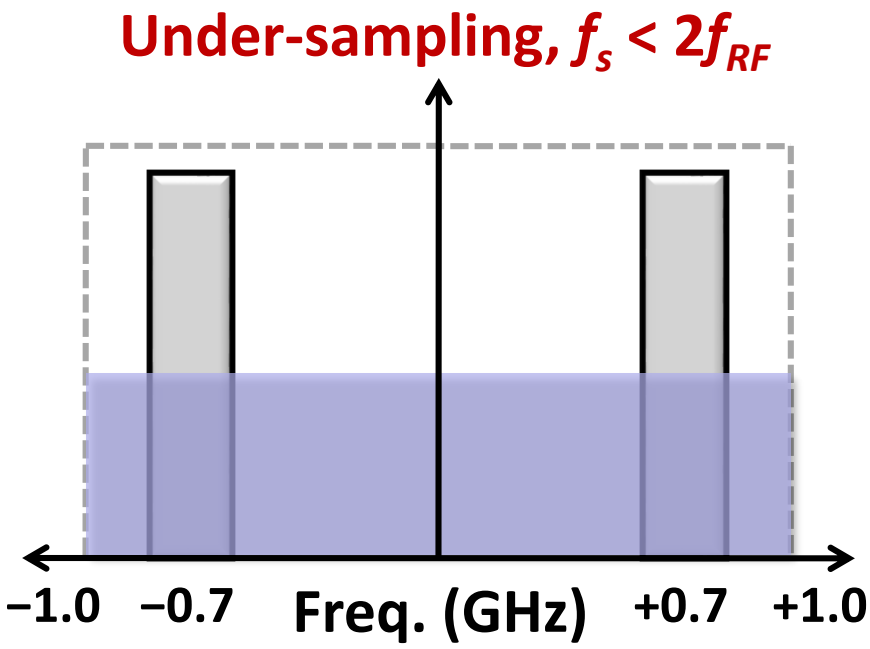
- **Widely varying dynamic range across standards**
  - GSM requires 84dB in 200kHz bandwidth
- **Ideal receiver meets the strictest constraint**
  - Design margin also required for wideband digitization



Under-Sampling

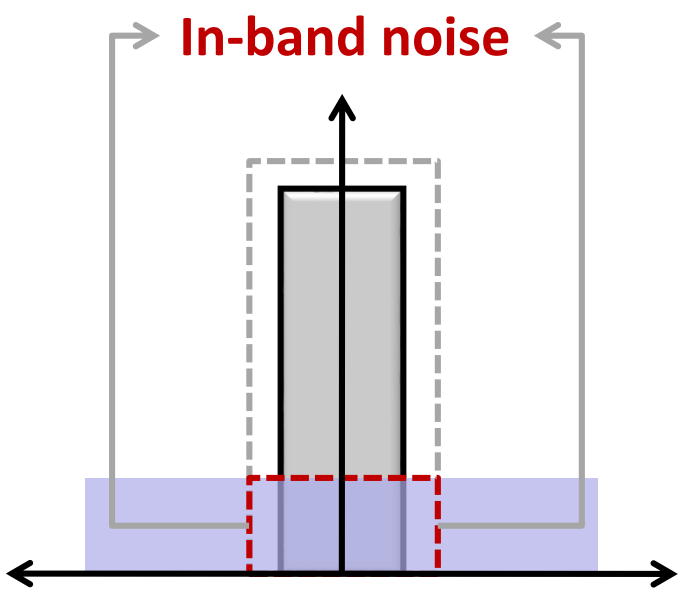
- **Nyquist criterion**
  - Sample the RF signals at $f_s > 2f_{RF}$
- **Sample at rate lower than Nyquist frequency**
  - Signal bandwidth << f_{RF}
  - Exploit aliasing, every f_s folds back to the baseband



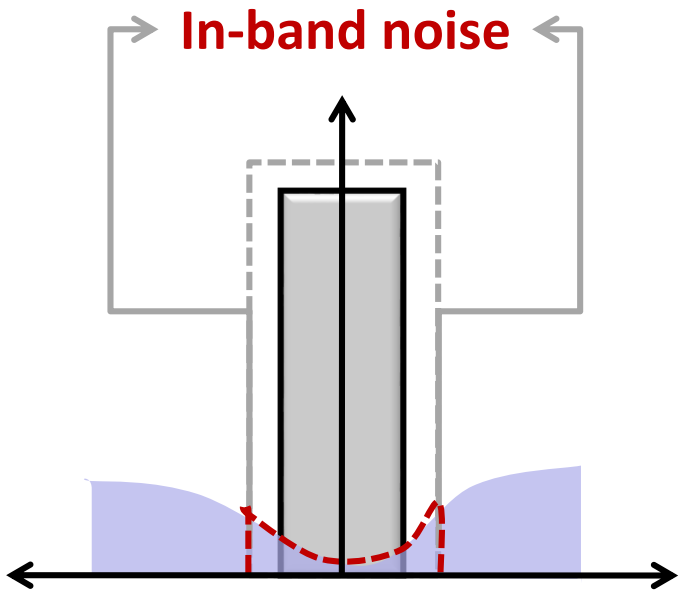


Sigma-Delta Modulation

- **Design constraints relax if number of bits in signal reduce**
  - Leads to more quantization noise
  - Sigma-delta modulation shapes the quantization noise
  - Noise is small in the signal band of interest



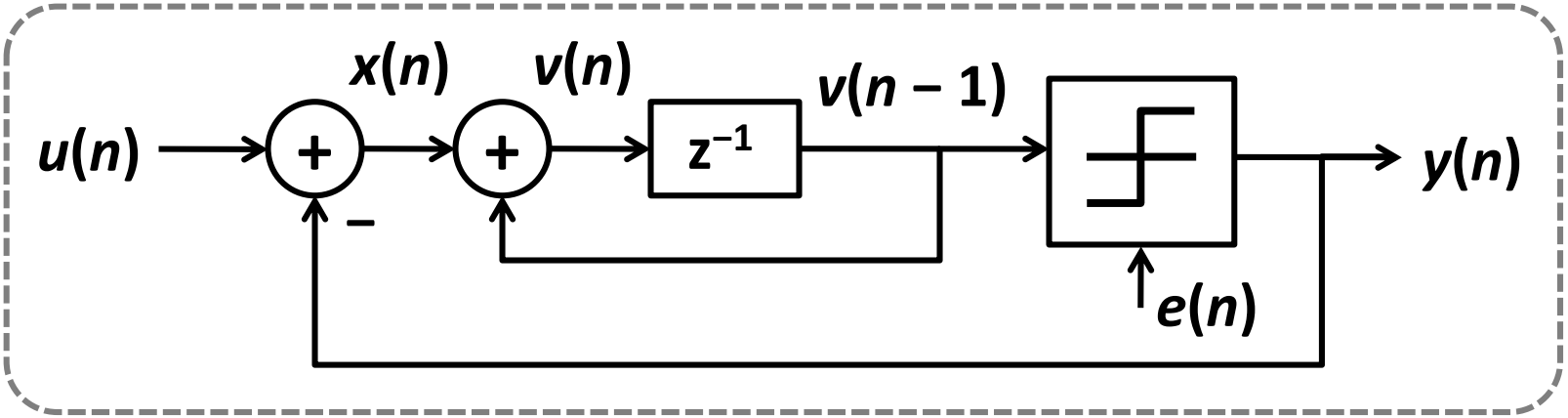
Flat quantization noise spectrum



Sigma-delta shaped quantization noise

Noise Shaping in Sigma-Delta Modulation

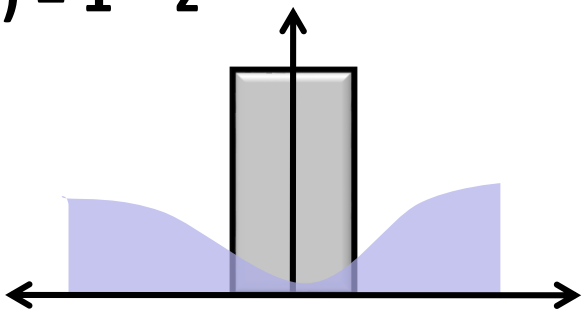
- **Quantization noise shaping for reduced number of bits**



$x(n) = u(n) - y(n)$
$v(n) = x(n) + v(n-1)$
$y(n) = v(n-1) + e(n)$
$v(n) = u(n) - e(n)$
$y(n) = u(n-1) + e(n) - e(n-1)$

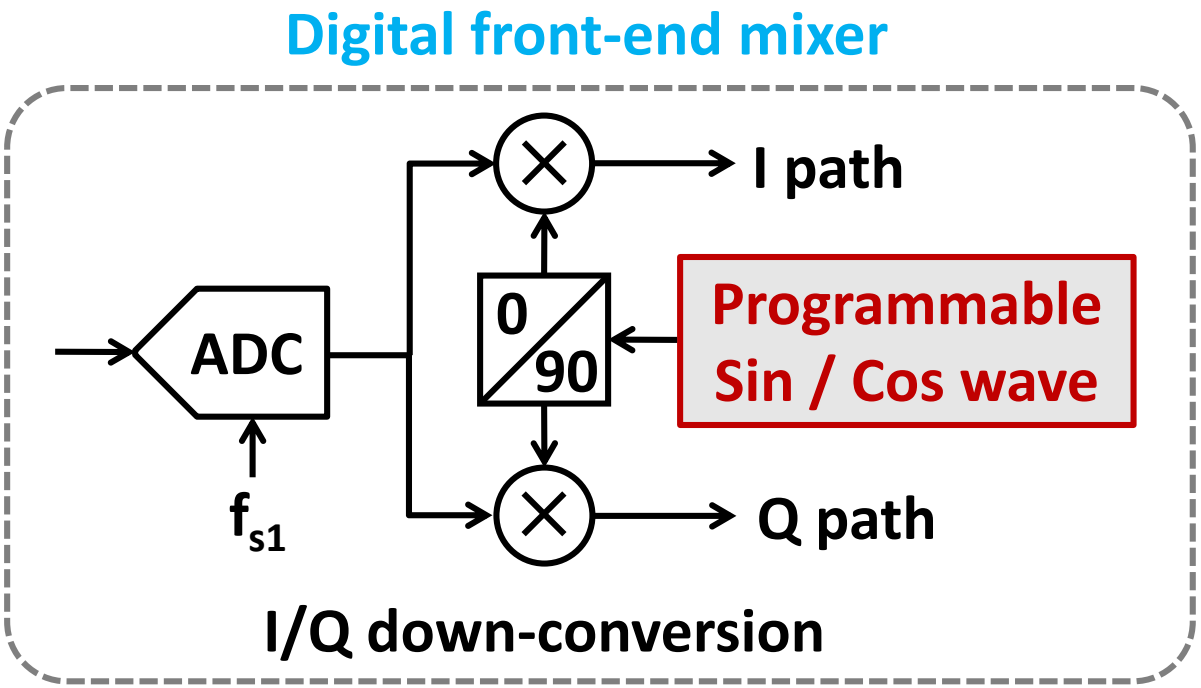
$$Y(z) = z^{-1}U(z) + E(z)\cdot(1 - z^{-1})$$

Noise shaping function 1st order,
$H(z) = 1 - z^{-1}$



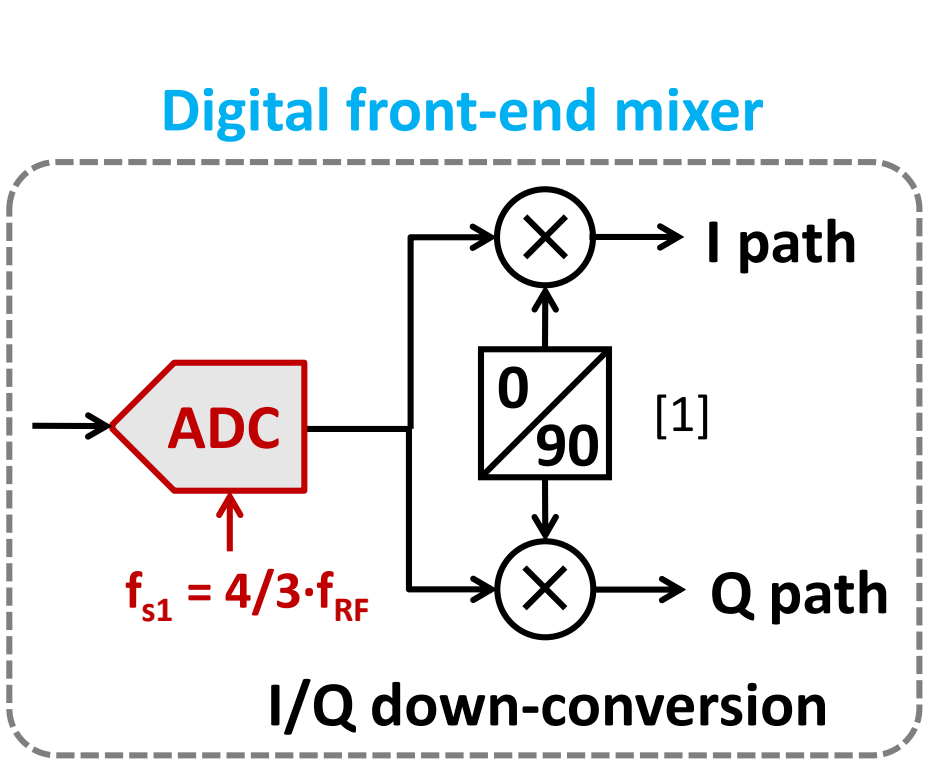
Quantization noise high-pass filtered

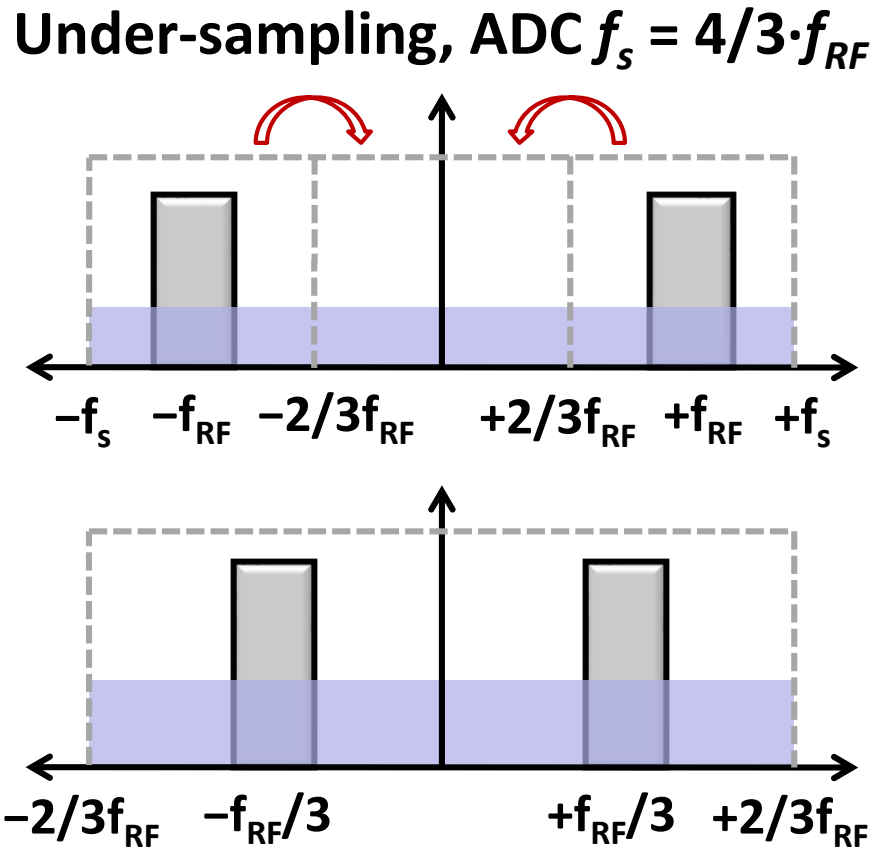
Carrier Multiplication



- **Multiplication with sine and cosine f_{RF}**
  - f_{RF} is arbitrary with respect to ADC sampling frequency f_{s1}
  - Mixer will be digital multiplier, infeasible at GHz frequency
  - Sine and cosine signals come from a programmable block
  - Carrier generation also not feasible at high f_{s1}

Optimized Carrier Multiplication

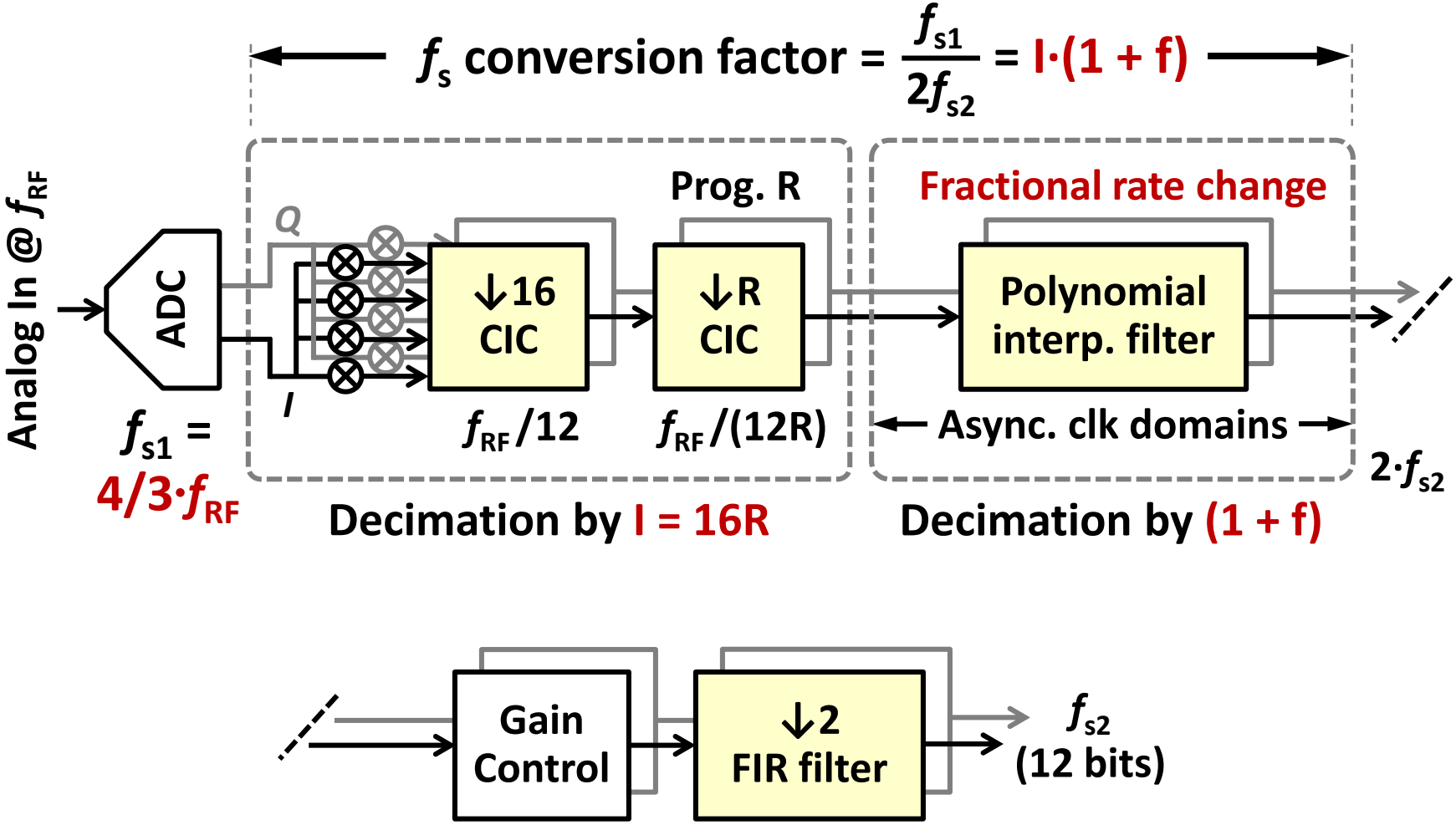




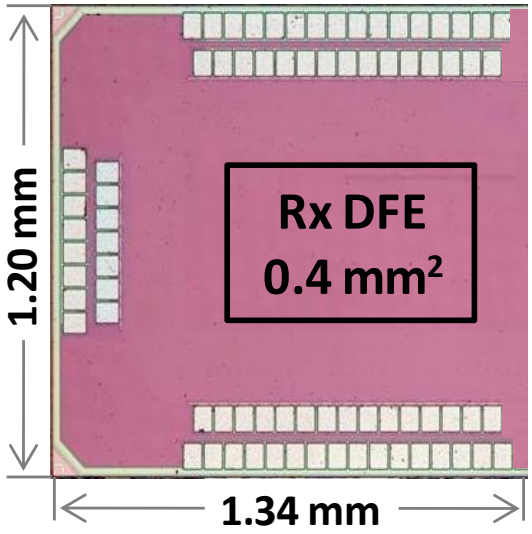
- **Choose $f_{s1} = 4/3 \cdot f_{RF}$**
  - Under-sampling of signal positions it at $f_{s1}/4 = f_{RF}/3$
  - Sine and Cosine signals for $f_{s1}/4 \in \{1,0,-1,0\}$

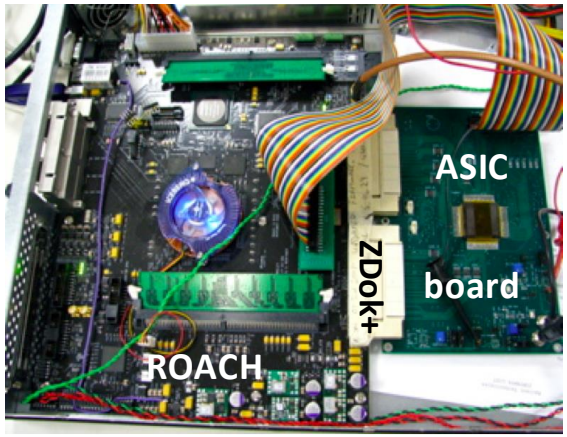
[1] N. Beilleau *et al.*, "A 1.3V 26mW 3.2GS/s Undersampled LC Bandpass ΣΔ ADC for a SDR ISM-band Receiver in 130nm CMOS, " in *Proc. RFIC Symp.,* June 2009, pp. 383-386.

Final RxDFE Architecture



RxDFE Chip Summary

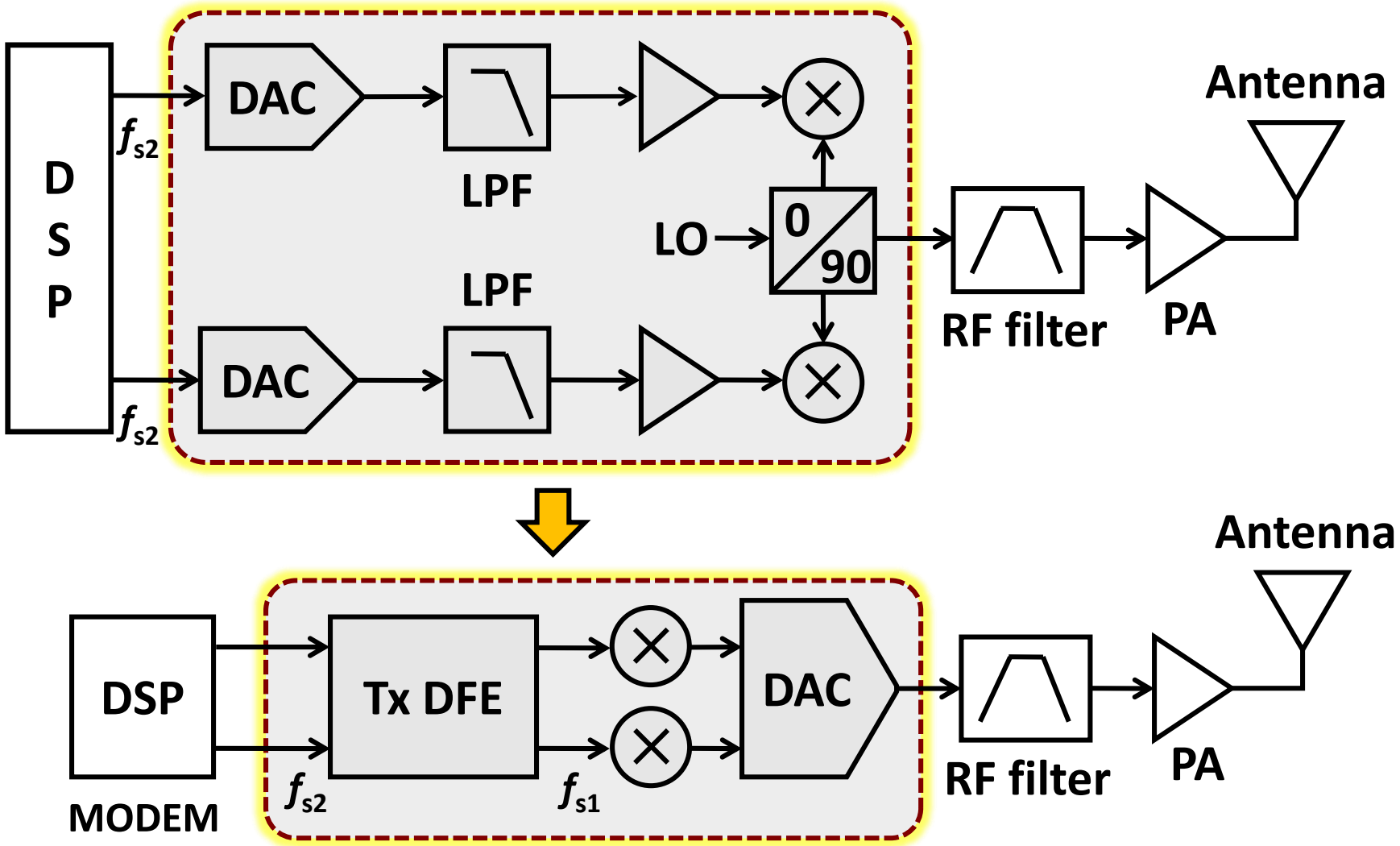




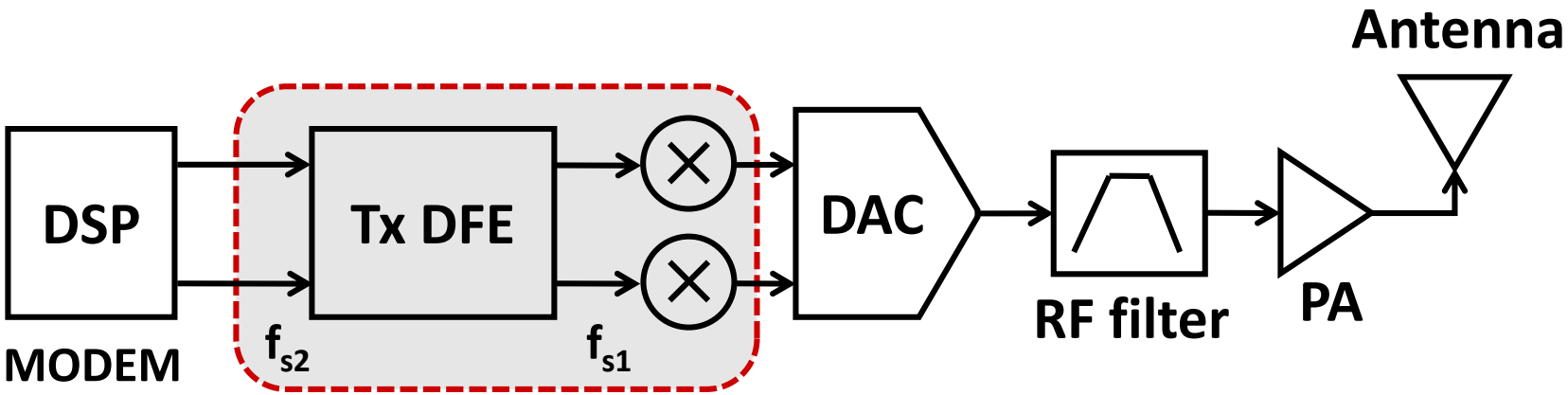
Reference	[1]	This work#
Technology	130 nm	65 nm
V_{DD}	1.5 V	1.0 V
Area	N/A	0.4 mm²
Max f_{s1}	104 MHz	2.7 GHz
Max f_{RF}	2.1 GHz	2.0 GHz*
Max BW	5 MHz	20 MHz
Max I(V_{DD})	21 mA	14 mA
Noise figure	9.2 dB	< 3dB

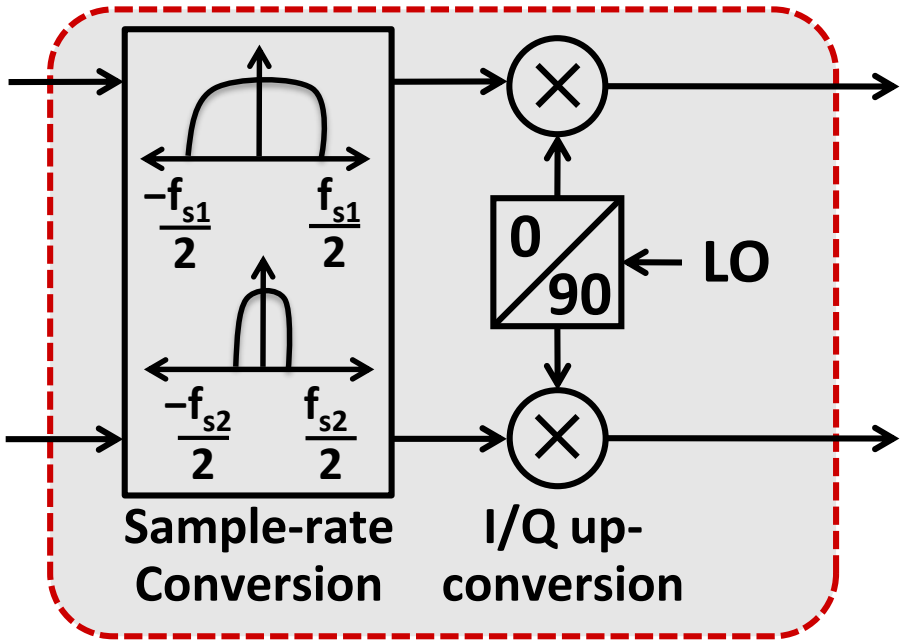
[1] G. Hueber, et al., RFIC 2008, pp. 25-28.
R. Nanda, et al., A-SSCC 2011, pp. 377-380.
* 2.025GHz (infrastructure limitations).

Digitizing Tx Front-End (TxDFE)



Tx DFE Functionality

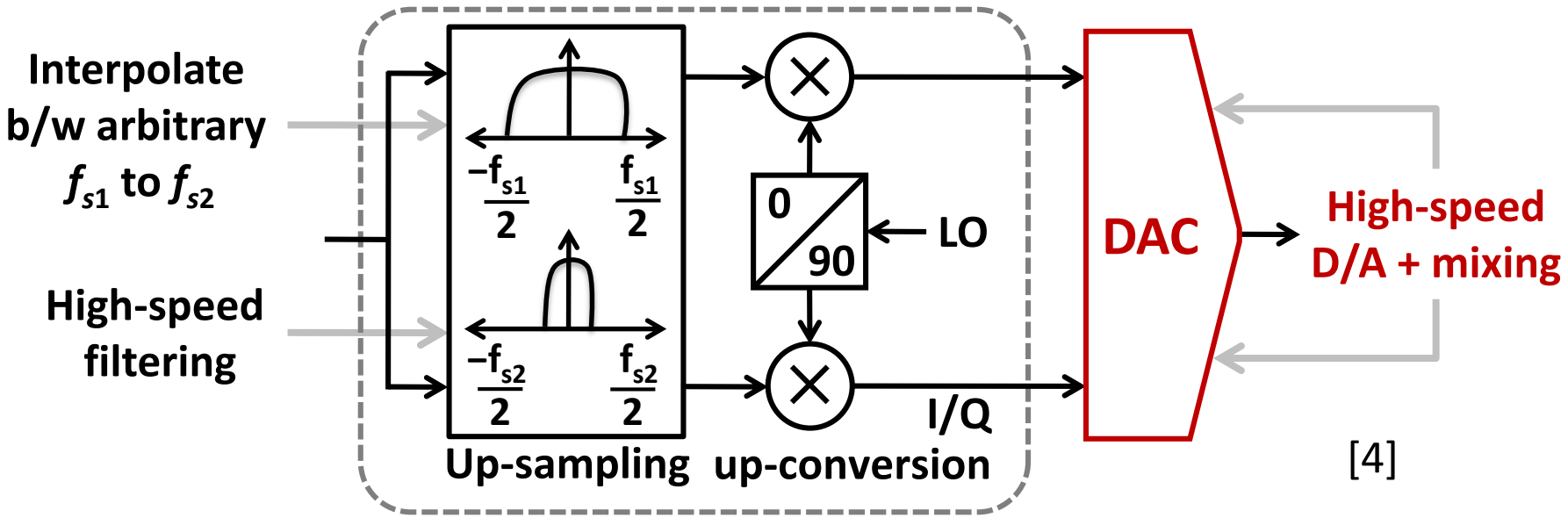




Convert from MODEM frequency f_{s1} to RF frequency f_{s2} while maintaining EVM

Tx DFE: Low-Power Design Challenges

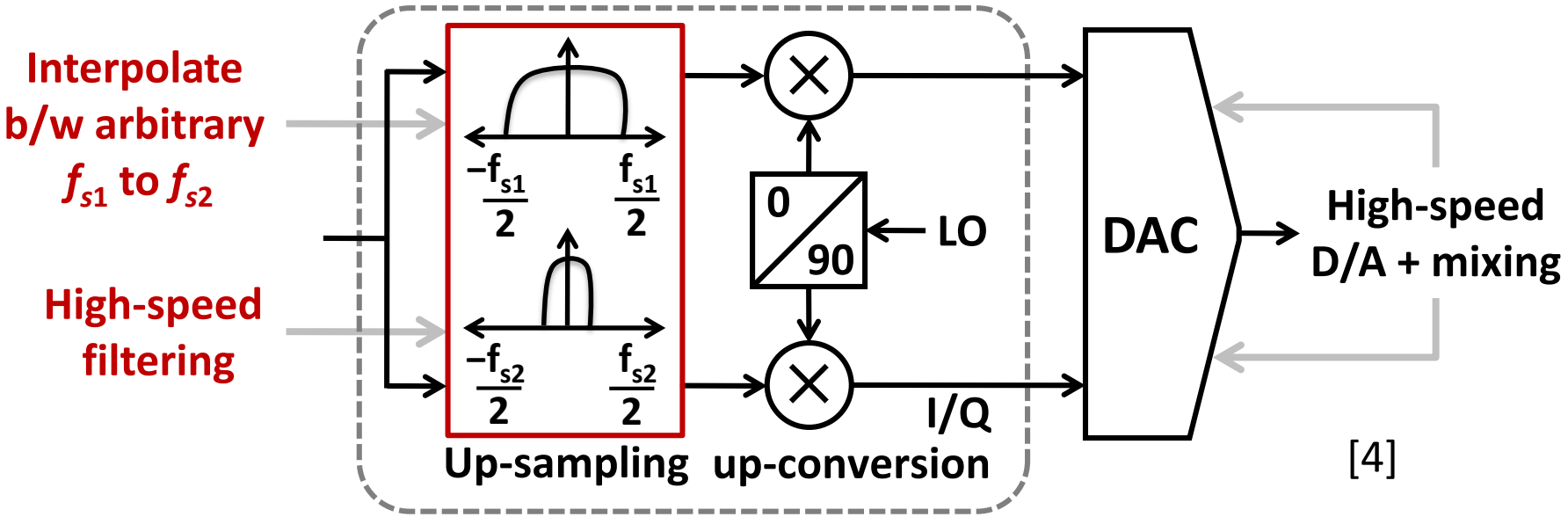
- **Challenge #1: DAC design**
  - High speed digital-to-analog conversion required



[4] P. Eloranta *et al.,* "A Multimode Transmitter in 0.13 um CMOS Using Direct-Digital RF Modulator," *IEEE J. Sold-State Circuits,* vol. 42, no. 12, pp. 2774-2784, Dec. 2007.

Tx DFE: Low-Power Design Challenges

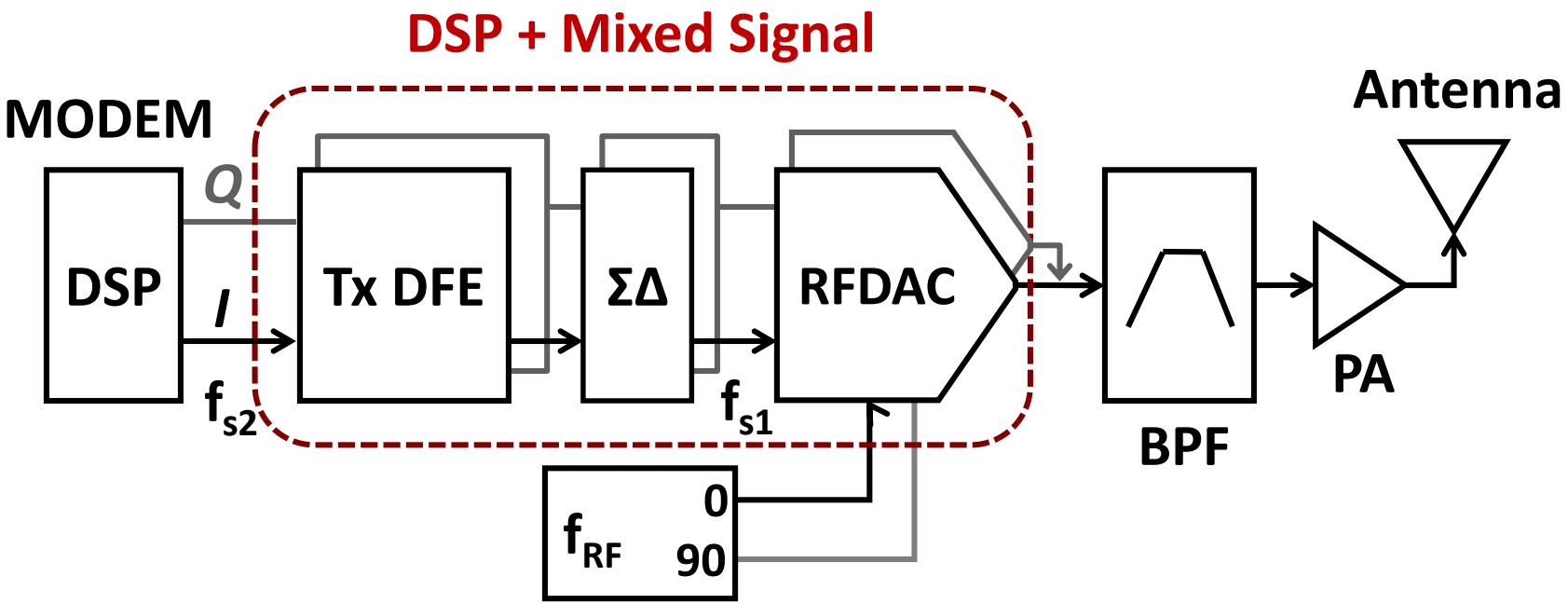
- **Challenge #2: Tx DFE design**
  - Carrier multiplication (digital mixing) at GHz frequencies
  - Anti-imaging filters before DAC function at GHz rates
  - Architecture must support fractional interpolation factors



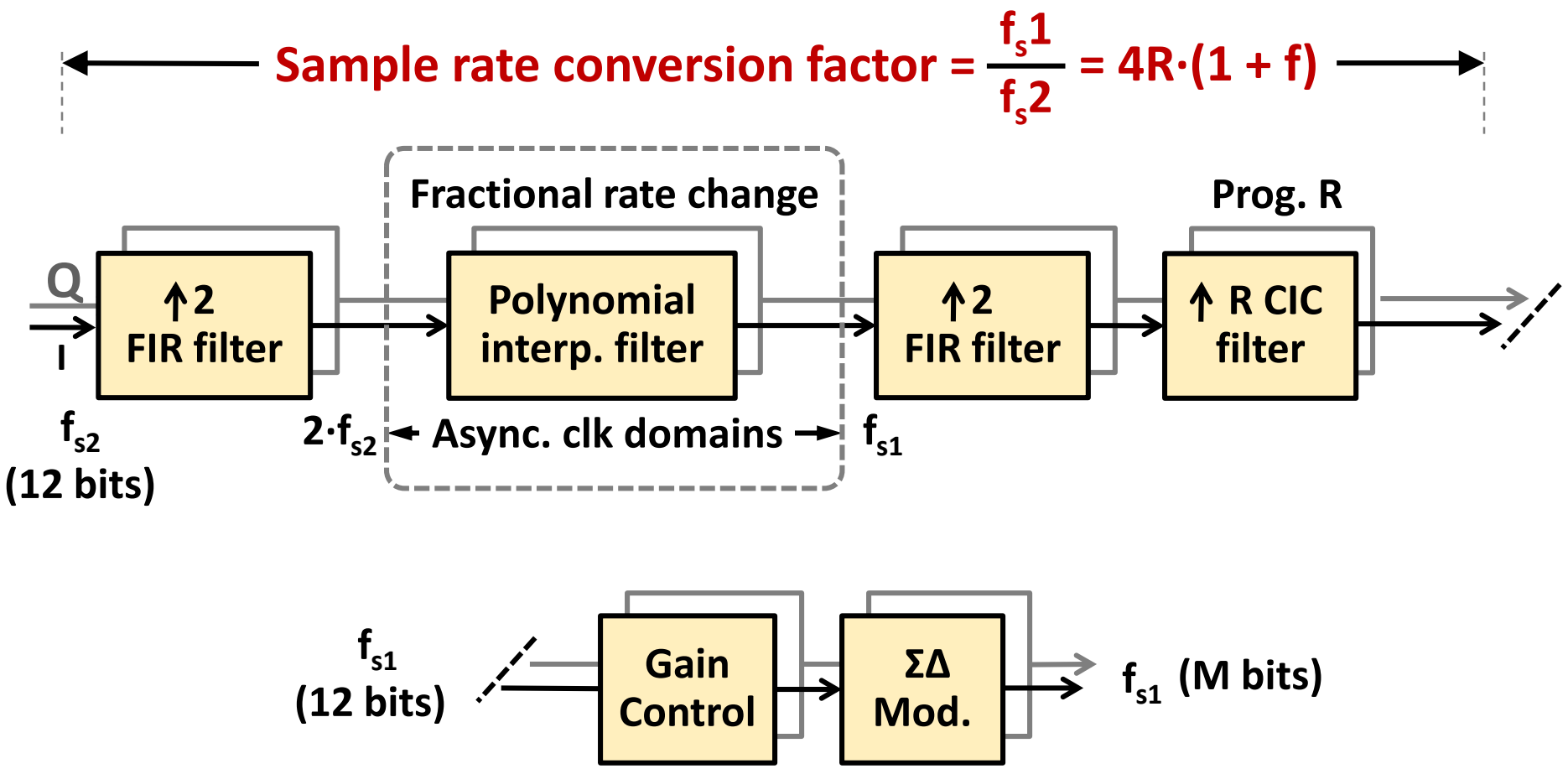
[4] P. Eloranta *et al.,* "A Multimode Transmitter in 0.13 um CMOS Using Direct-Digital RF Modulator," *IEEE J. Sold-State Circuits,* vol. 42, no. 12, pp. 2774-2784, Dec. 2007.

Transmitter Front-end

- Tx DFE upsamples and lowpass filters baseband signal
- ΣΔ modulator compresses wordlength of DAC input
- RFDAC is a mixer and D/A converter

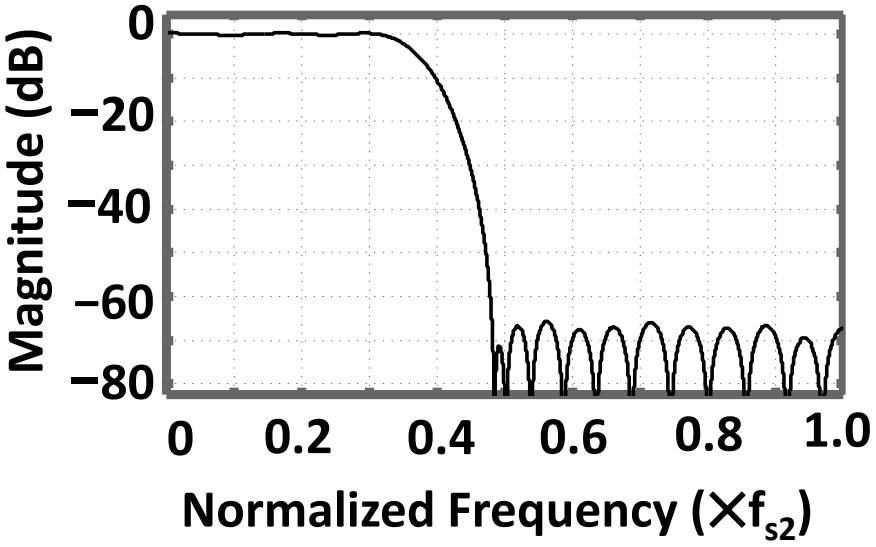


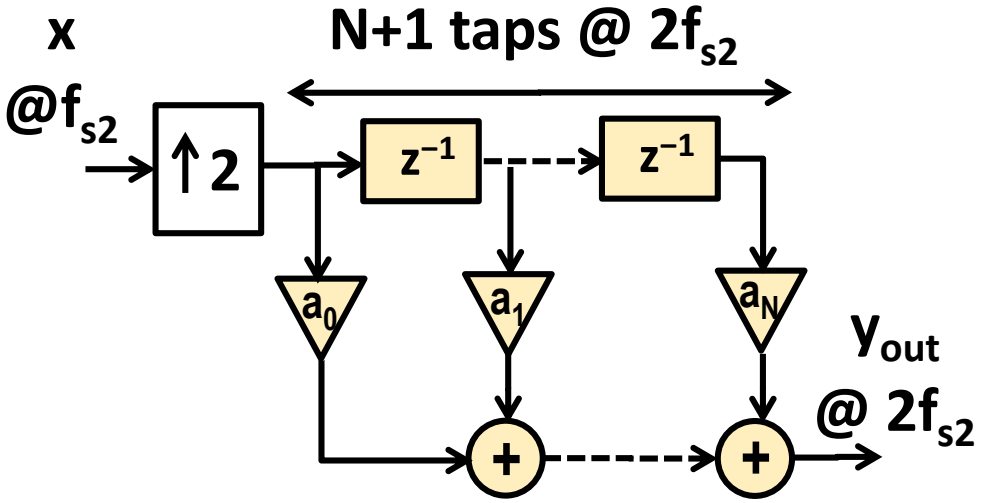
Tx Digital Front-end (DFE)



FIR Interpolator

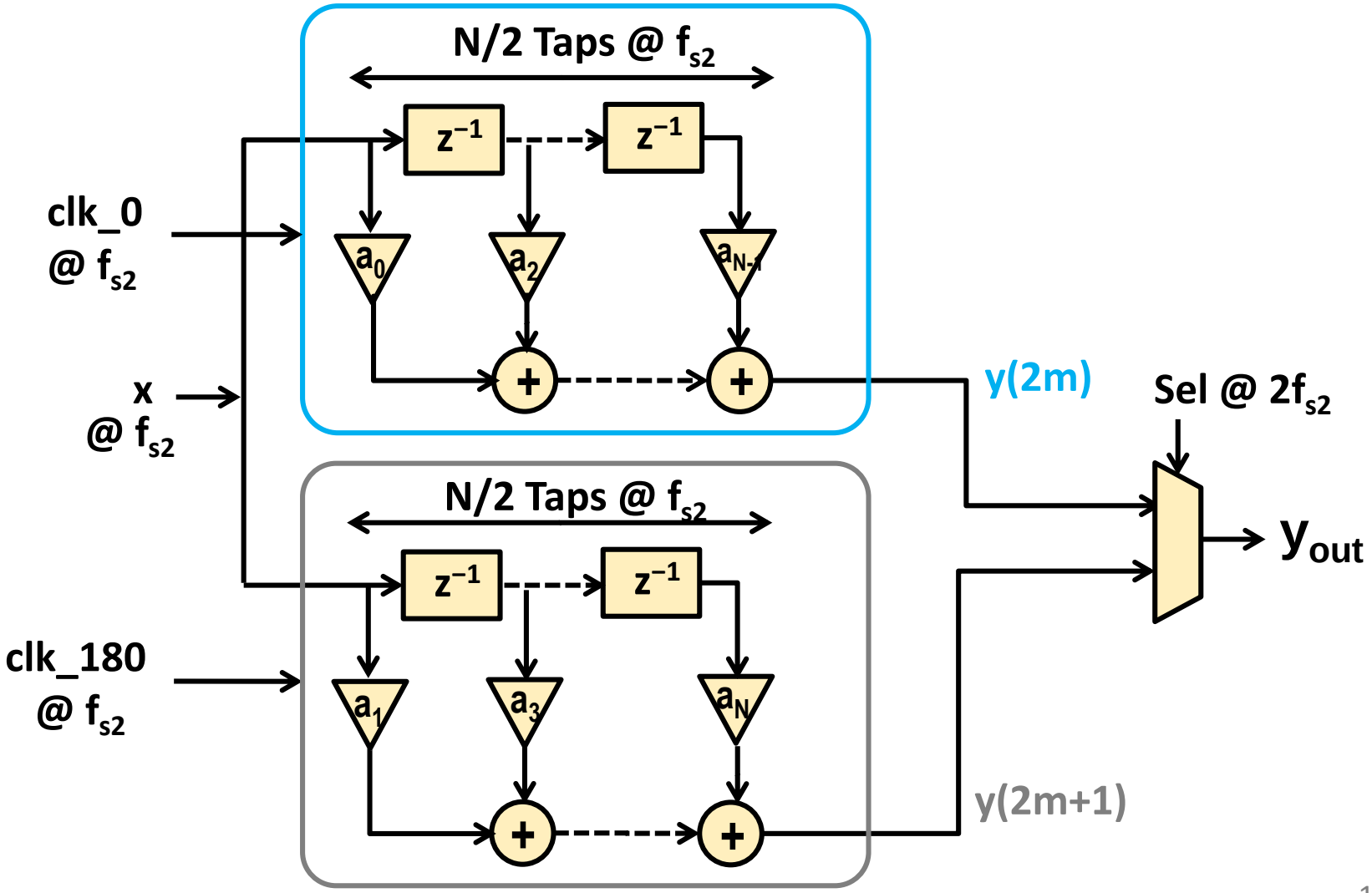
- **Upsamples and lowpass filters by a factor of 2**
- **Target attenuation**
  - Determined by adjacent channel power ratio (ACPR)
- **Can be made fixed or with reconfigurable taps**





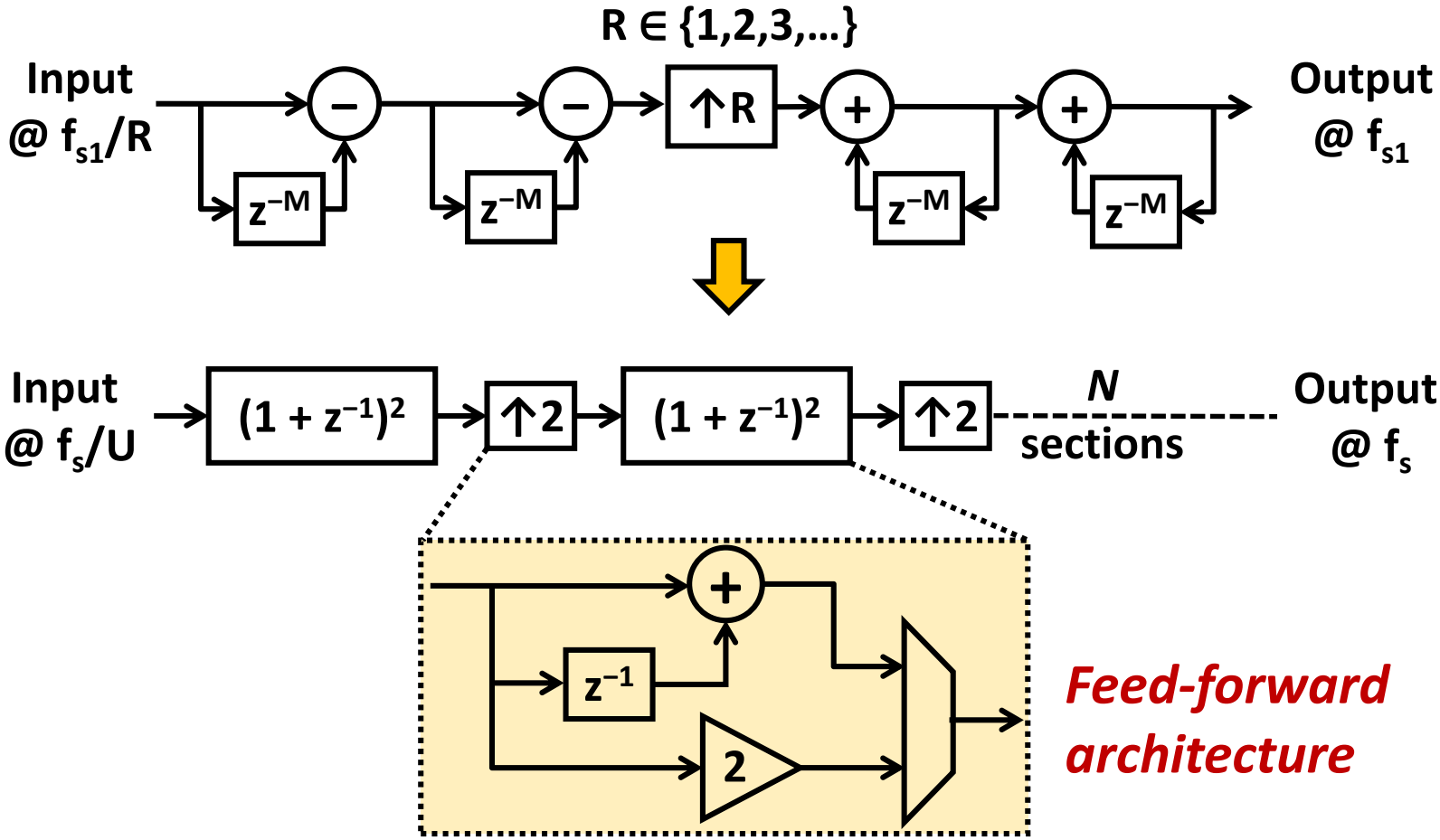
FIR Interpolator Optimization

Poly-phase implementation, operating at f_{s2}



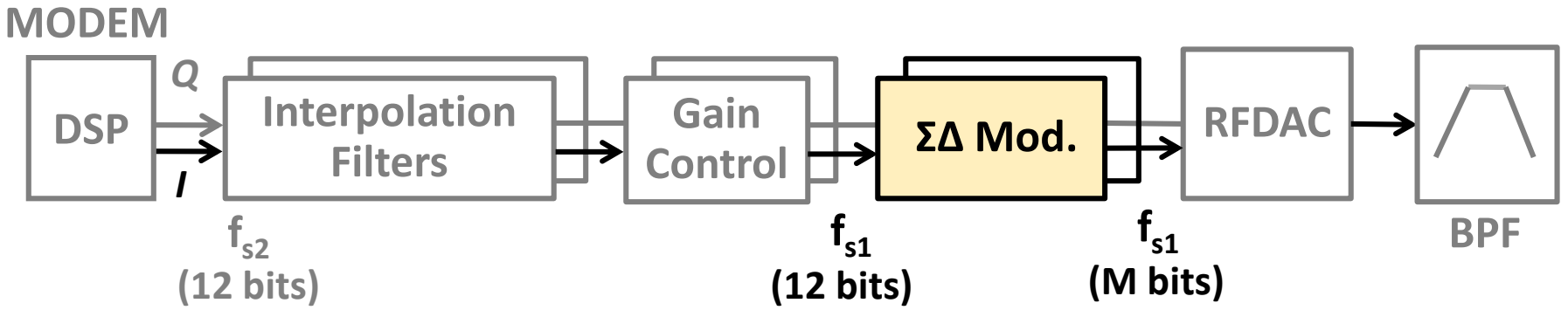
CIC Interpolator Optimization

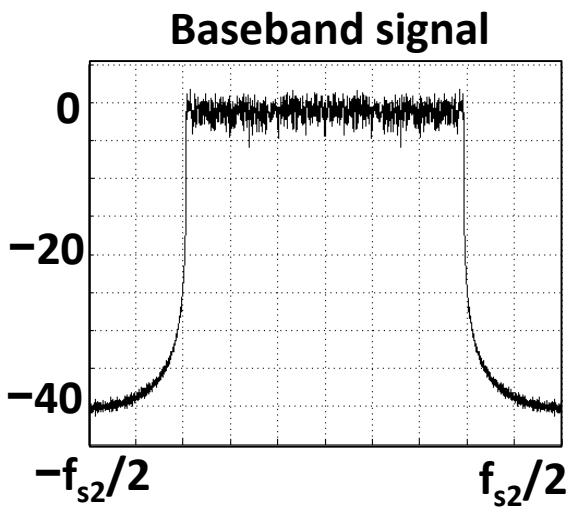
- Shorter WL
- Pipelning, parallelism in feedforward architecture

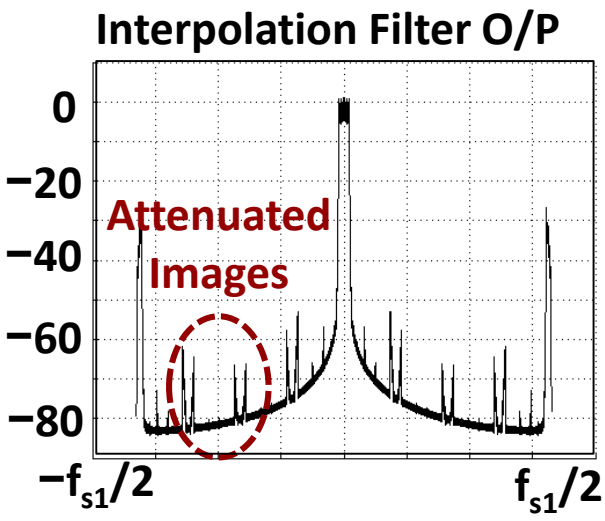


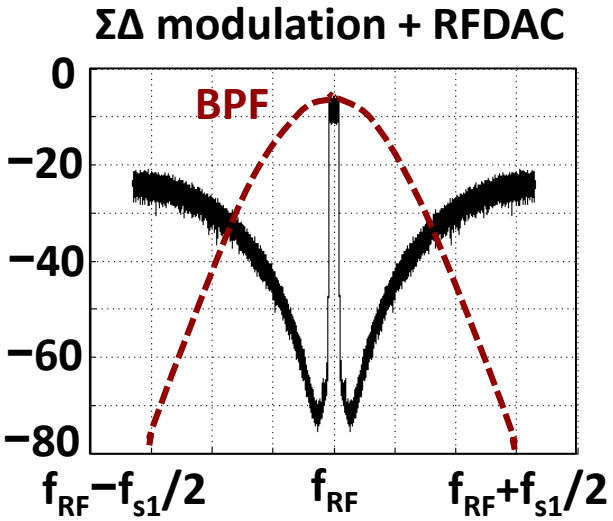
Compression with ΣΔ Modulation

- 12-bit wide signal from interpolation filters
- ΣΔ modulator compresses signal to M bits (M < 12)



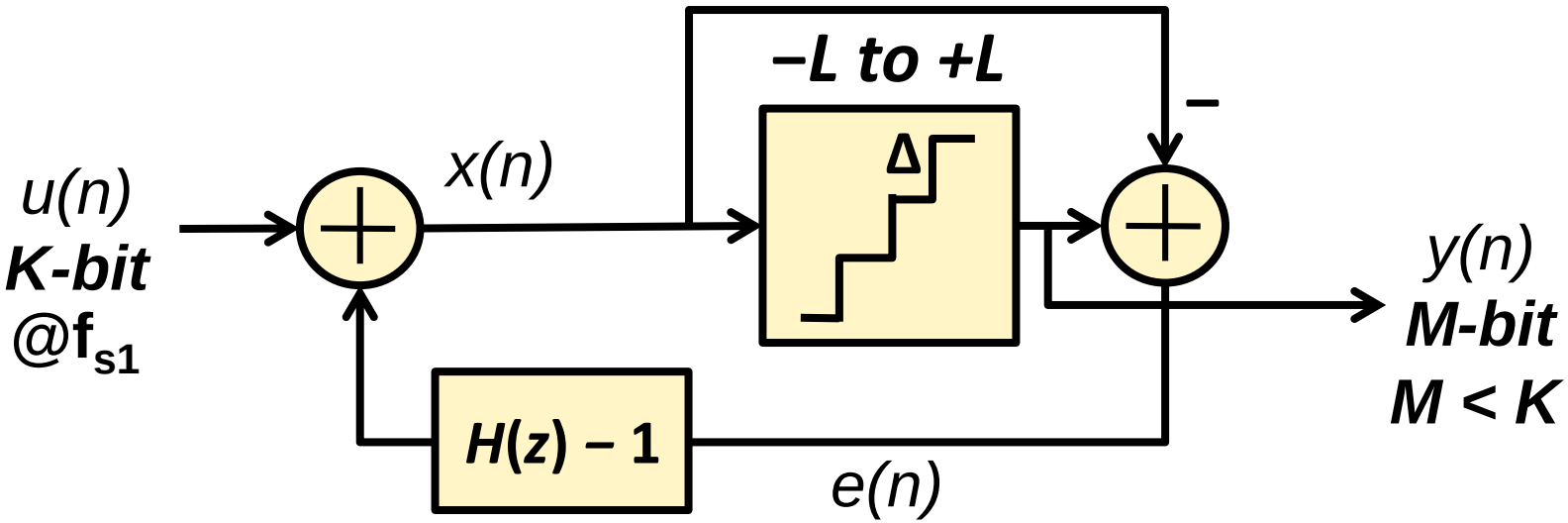






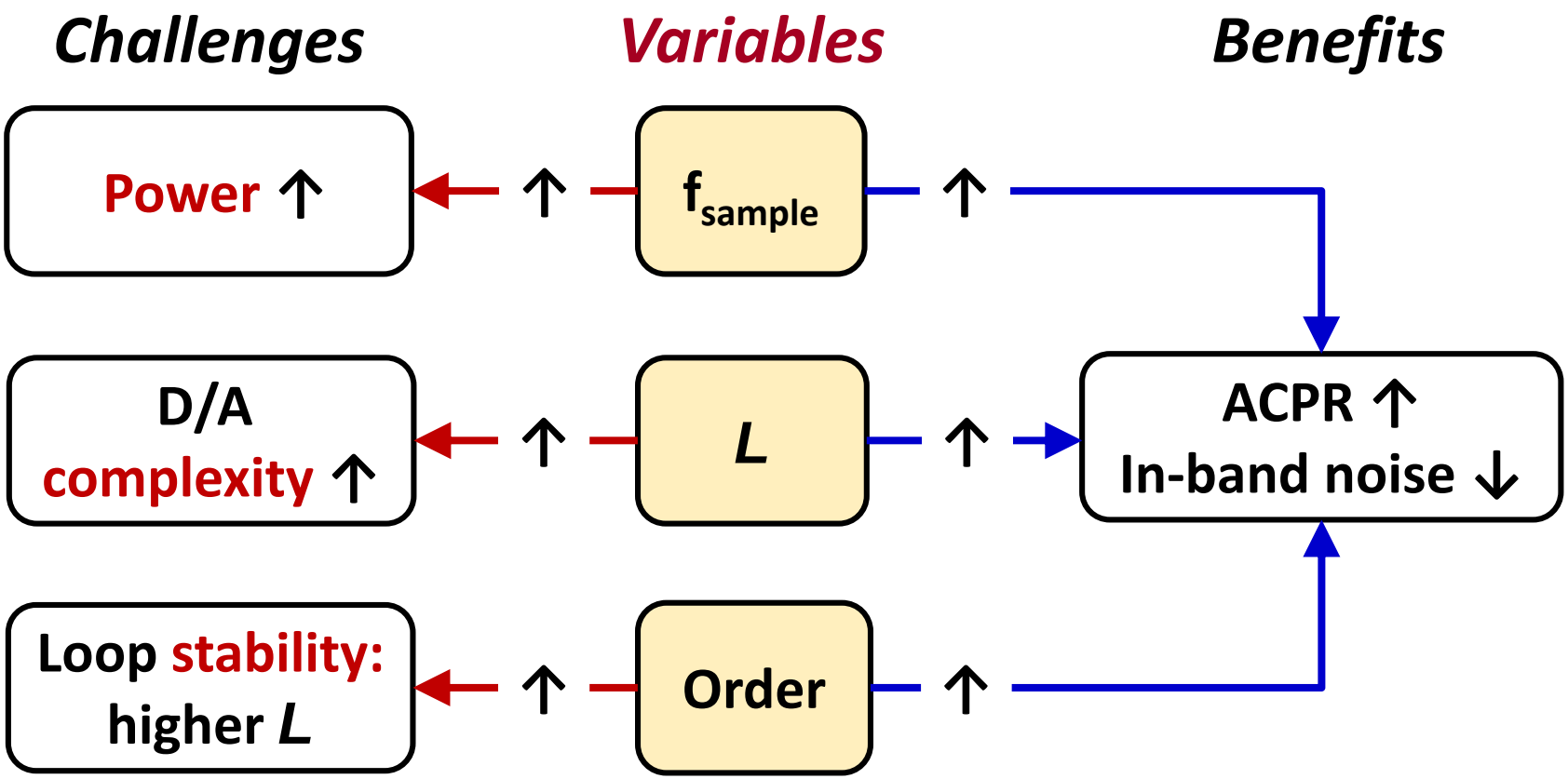
ΣΔ Modulator Topology

- **Noise shaping coder topology**
  - H(z): Noise shaping function
- **Design variables: f_{s1}, L, H(z)**



$$E(z) = Y(z) - X(z)$$
$$X(z) = U(z) + (H(z) - 1)E(z)$$
$$Y(z) = U(z) + H(z)E(z)$$

ΣΔ Modulator Tradeoffs



High-order low-f_{sample} ΣΔ for overall lower power

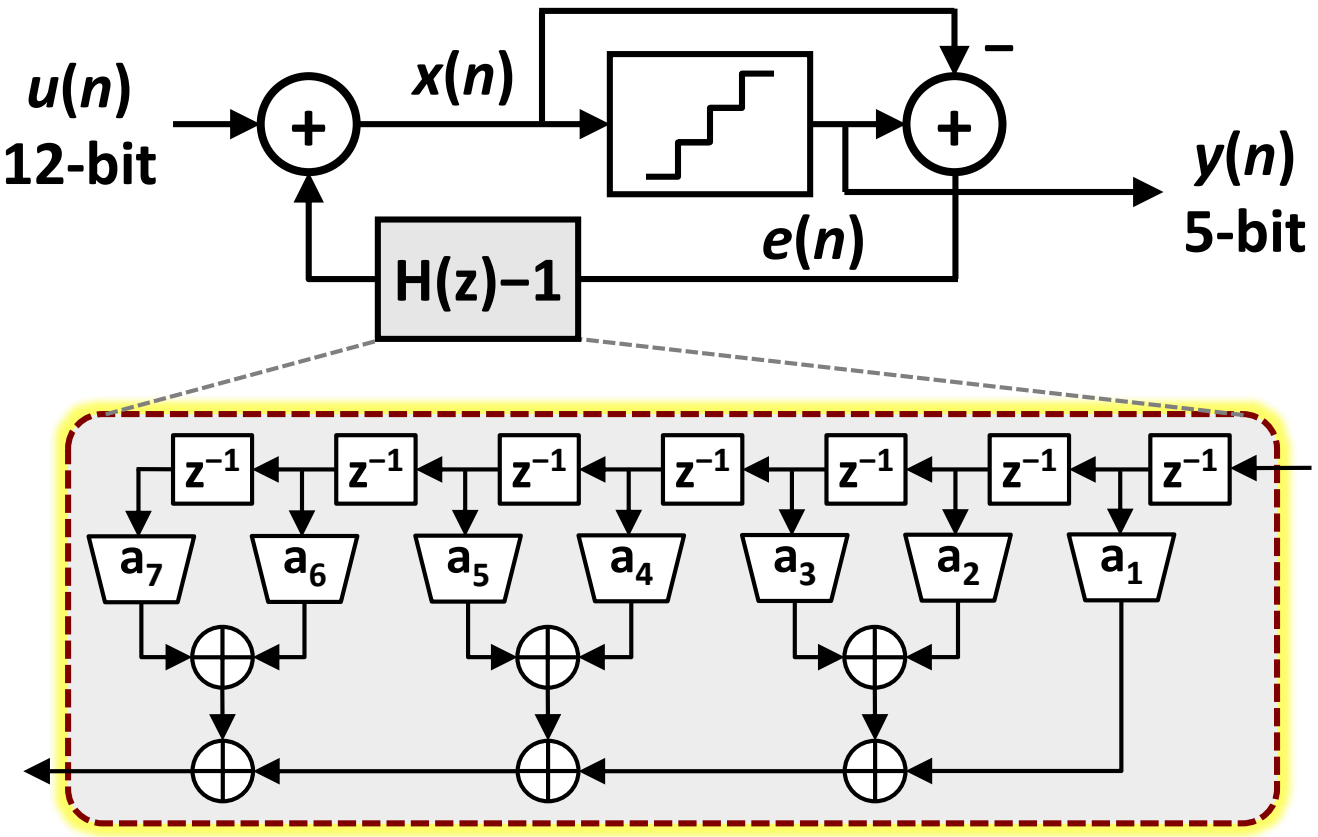
Previous Work

- **Low-order modulation, high f_{sample}**
- **High digital power consumption**

[1] A. Jerng, et al., JSSC 08/07.
[2] P. Eloranta, et al., JSSC 12/07.
[3] A. Pozsgay, et al., ISSCC 2008.
[4] A. Frappé, et al., JSSC 09/09.

Reference	[1] 2007	[2] 2007	[3] 2008	[4] 2009
ΣΔ modulator	**2nd order**	**-**	**3rd order**	**3rd order**
DAC structure	3-bit DRFC	10-bit DRFC	6-bit DRFC	1-bit
Sample rate (f_s)	**2.625 Gs/s**	**307.2 Ms/s**	**5.4 Gs/s**	**4 Gs/s**
RF carrier (max)	5.25 GHz	1.9 GHz	2.7 GHz	1 GHz
Bandwidth	200 MHz	5 MHz	20 MHz	50 MHz
ACPR	-	55 dB	43 dB	53.6 dB
EVM	-	< 2%	2.1%	1.24%
Power	**187 mW**	**157 mW**	**190 mW**	**120 mW**
Area	0.72 mm^2	1 mm^2	0.8 mm^2	0.15 mm^2
Process	130 nm	130 nm	65 nm	90 nm
Flexible f_s and f_{RF}	**No**	**Yes**	**Yes**	**No**

7th Order ΣΔ Modulator

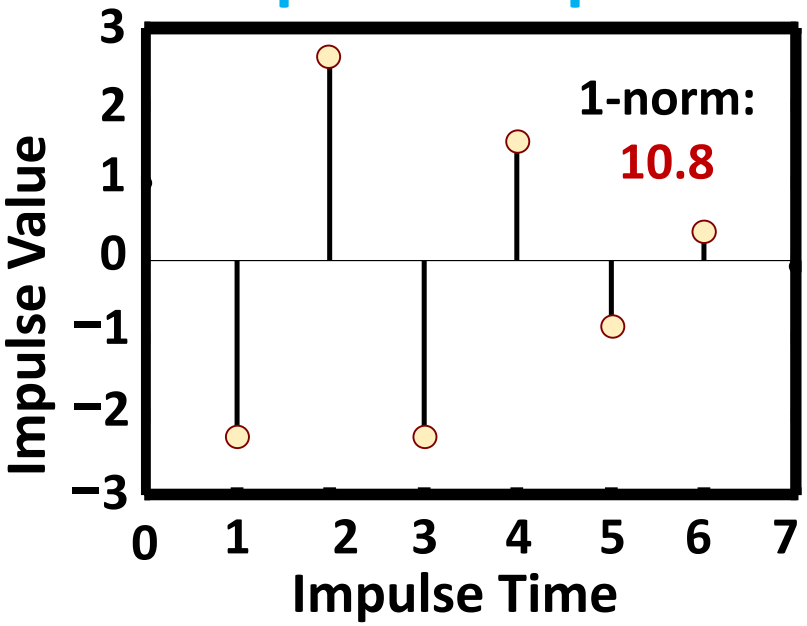


- **Challenge:** Stabilize NTF loop
- Lower f_{sample} and power

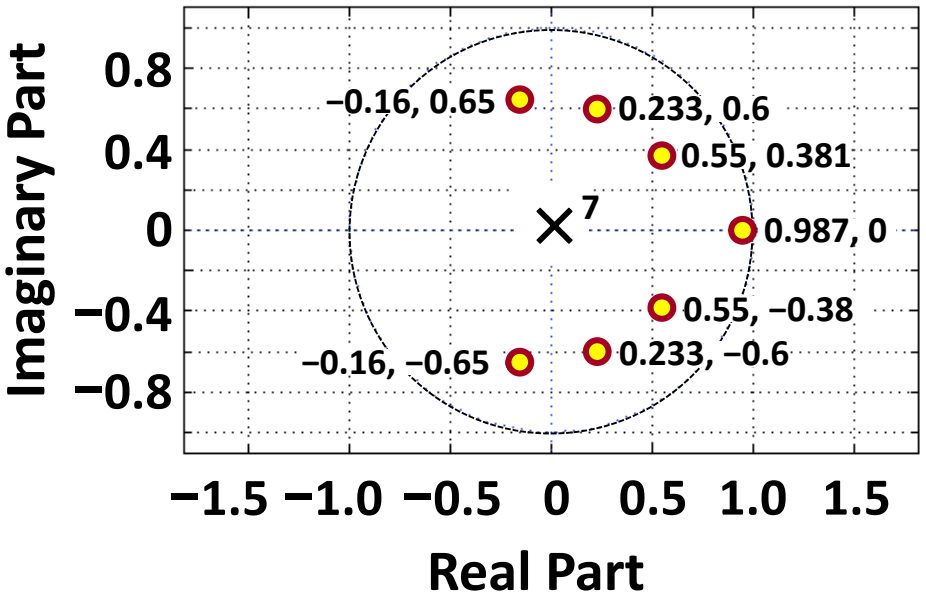
Min-phase FIR for Loop Stability

- **Min-phase FIR: lowest 1-norm** for a magnitude response
- **Lowest 1-norm: loop stability** with minimum number of quantization levels for a given input

Impulse Response

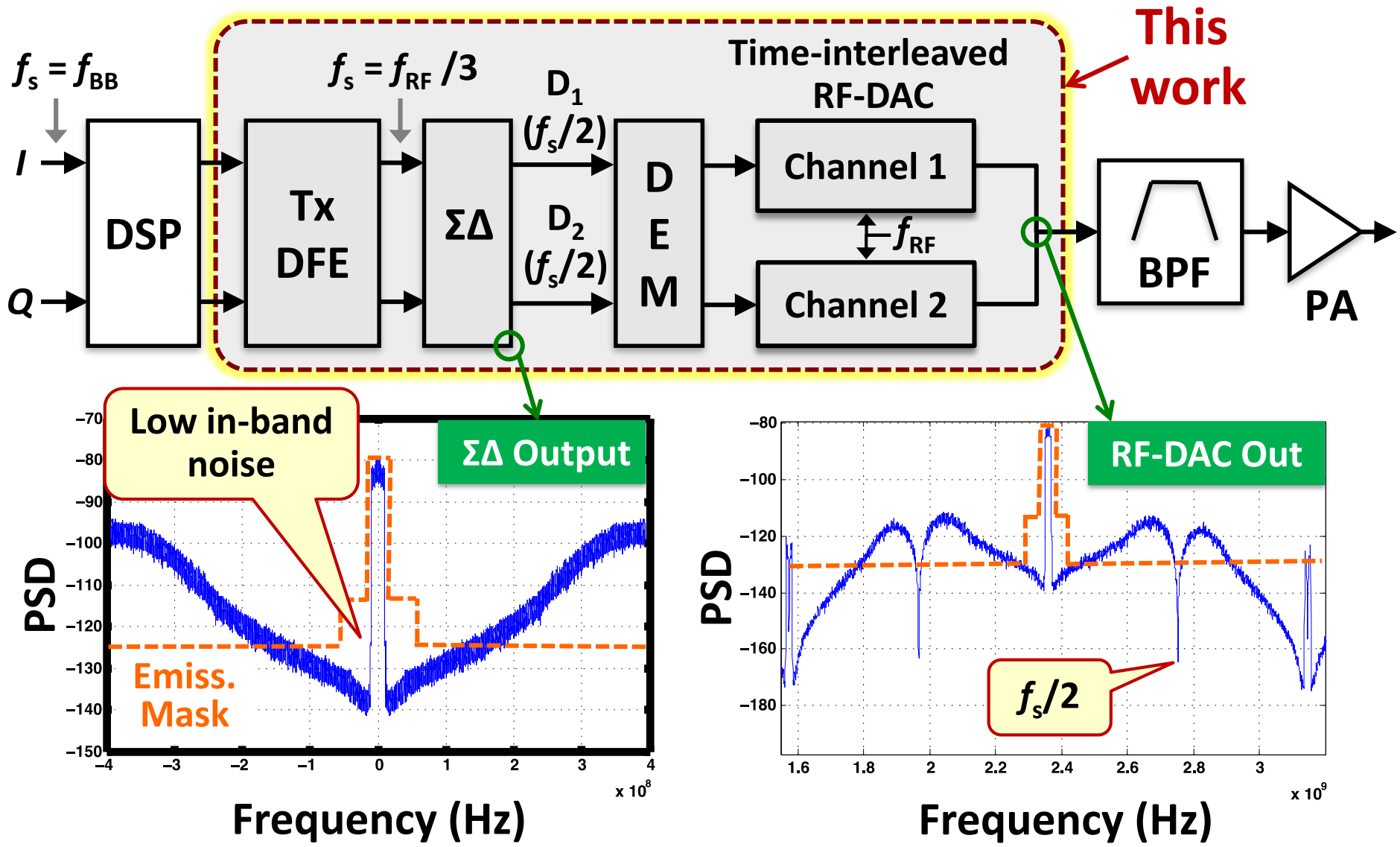


Pole/Zero Plot



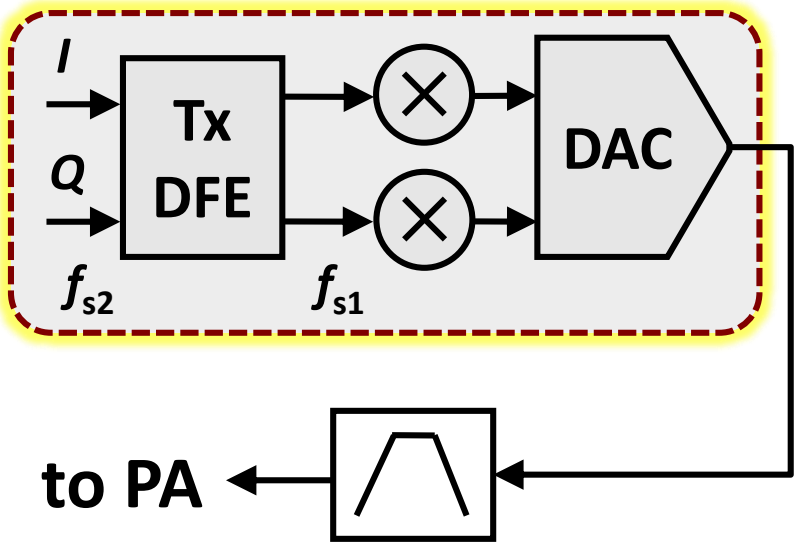
S. Norsworthy, ISCAS 1993, pp. 1353-1355.

ΣΔ Modulator & TI RF-DAC



Implication: Low-Q BPF

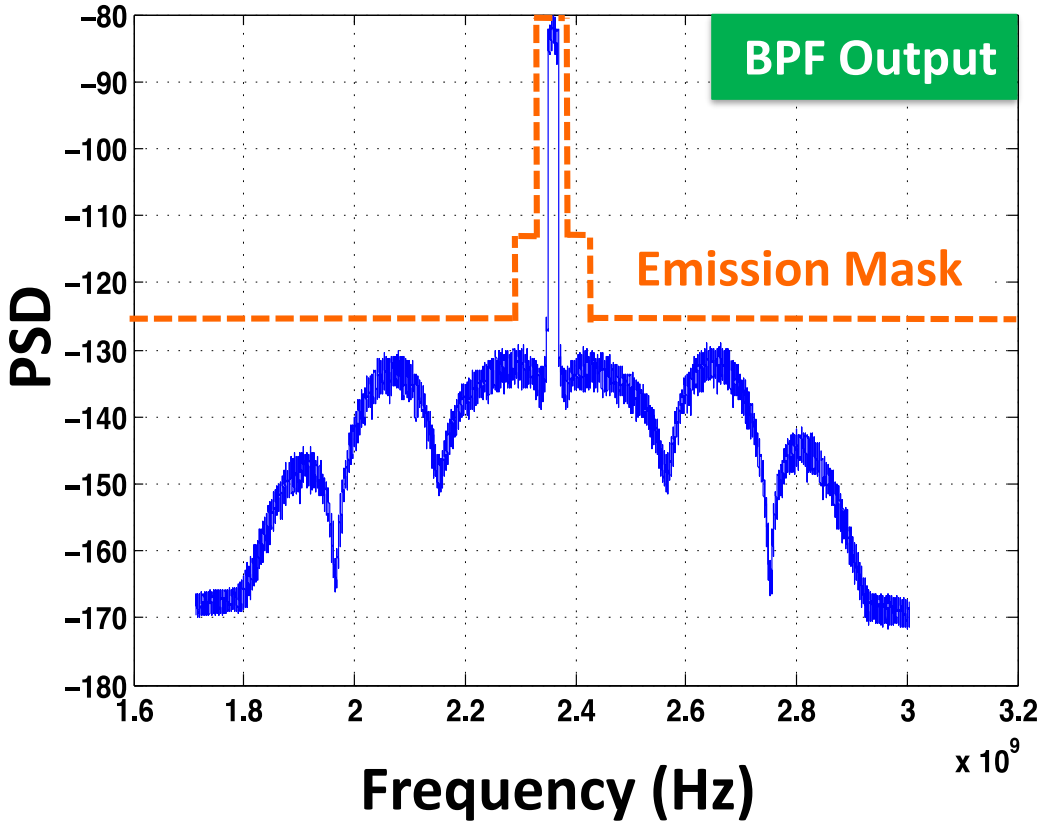
- Attenuates remaining quantization noise
- A 6th order BPF with Q = 7.7 is sufficient
  (3-pole)



BPF filter

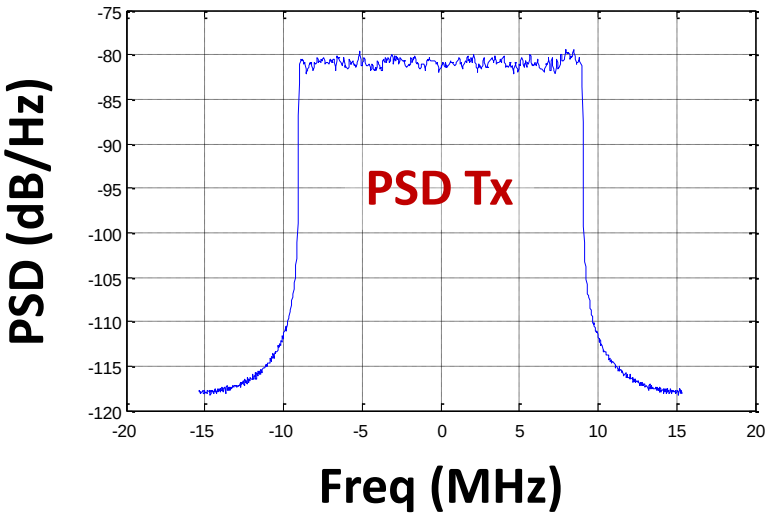
Q = 7.7

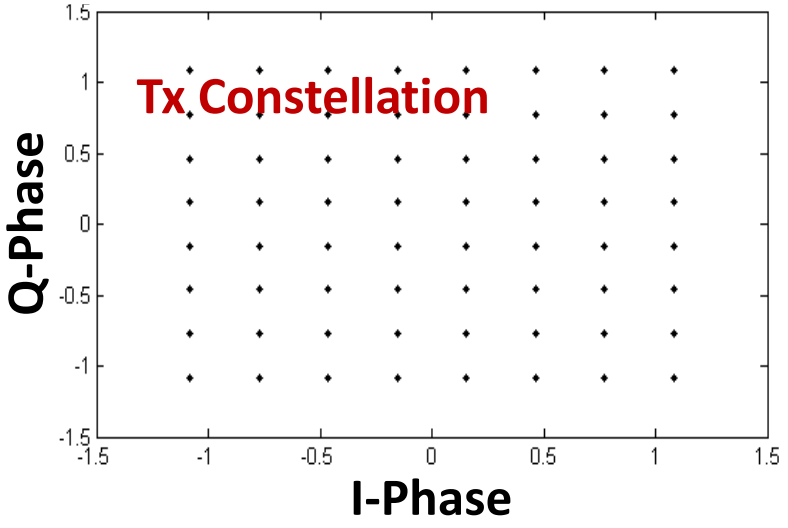
Could be re-optimized with
1-pole in below-65nm tech.

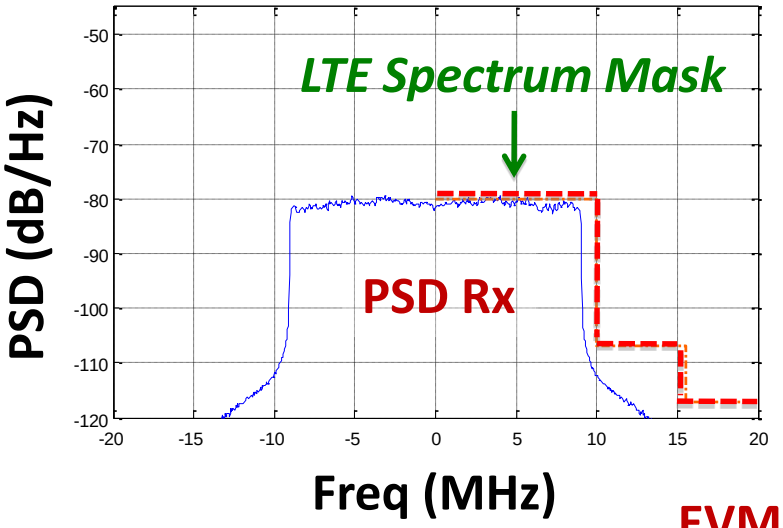


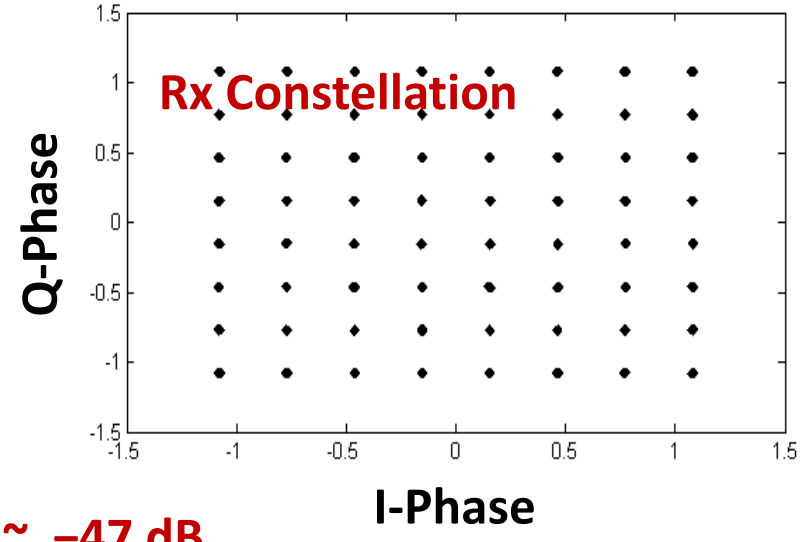
Tx DFE Functionality

Input from baseband modem quantized with 12 bits









EVM ~ –47 dB

Performance Comparison

Reference	[2] P. Eloranta, et al., JSSC 12/07.	[3] A. Pozsgay, et al., ISSCC 2008	This approach*
ΣΔ modulator	-	**3rd-order**	**7th-order**
DAC structure	10-bit DRFC	6-bit DRFC	5-bit DRFC
Sample rate (f_{s1})	307.2 MS/s	**5.4 GS/s**	**900 MS/s**
RF carrier (max)	1.9 GHz	2.7 GHz	2.7 GHz
Bandwidth	5 MHz	20 MHz	5 MHz
ACPR	55 dB	42.8 dB	42.5 dB
EVM	< 2%	2.1%	2.8%
O/P channel power	−9 dBm (64-QAM)	−8 dBm (64-QAM)	−8.1 dBm (64-QAM)
Power	157 mW (@ 1.9GHz)	**150 mW** (@ 2.4GHz)	**85.5 mW** (@ 2.4GHz)
Area	1mm^2	0.8mm^2	0.8mm^2
Technology	130nm	65nm	65nm
DEM	No	**No**	**Yes**
Flexible f_{s1}, f_{s2}	No	**Yes**	**Yes**

Summary

- **Digital front-end implementation**
  - Avoids analog non-linearity
  - Power and area scales with technology
- **Challenges**
  - High dynamic range ADC in receiver
  - High throughput at Rx input and Tx output
  - Minimum SNR degradation of received signal
  - Quantization noise and image suppression at Tx output
- **Optimization**
  - Sigma-delta modulation in Rx ADC
  - Sigma-delta NTF Optimization in Tx modulator
  - Filter optimization for low power operation (FIRs, CICs)