EE 140/240A Prof. Pister
Spring 2020

Homework Assignment #2v2

Due by online submission Thursday 2/6/2020 (late Friday at 9am)

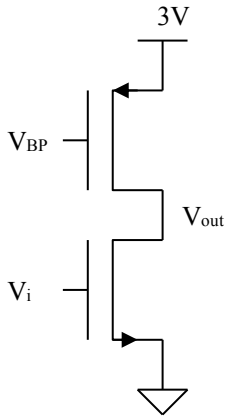
1. [not graded] How much does V_{TH} change if the temperature changes by 1 Kelvin? What is the range of thermal voltage over the industrial temperature range, -40 to +85 C?
2. Do this problem without using a calculator. You have a bag full of identical diodes. You measure one and find that it will pass 1uA when a voltage of 600 mV is applied at room temperature.
   a. if you apply 626 mV at room temperature, what do you expect the current to be?
   b. if you apply 660 mV at room temperature, what do you expect the current to be?
   c. if you use a current source to push 1nA through the diode at room temperature, what voltage do you expect to see?
   d. If you put 10 diodes in series and run 1 uA through them, what voltage do you expect to see across all 10 diodes?
   e. If you put 10 diodes in parallel and run 1 uA through the parallel combination, what voltage do you expect to see?
3. A PNP transistor has its collector at ground and its emitter at 10V. Assume that the current in the base-emitter diode is 1μA with 0.5V applied,
   a. What is the base voltage necessary to get a collector current of 1mA?
   b. Is the collector current due to the flow of mostly holes or electrons?
   c. If the collector voltage is raised, what is the maximum collector voltage that keeps the collector-base junction reverse biased?
   d. If the collector voltage is raised another 300mV so that the collector-base junction is forward biased, the collector current doesn't change much. Why?
4. [not graded] Using the datasheet from the Eimac 4-1000A vacuum tube that I showed you in class, if the tube is operating with 5,000 V on the plate and 0 V on the grid
   a. Estimate the plate current
   b. Estimate g_m, r_o, and the maximum possible gain for the tube used with a constant current source

   In a tube, the plate is sort of like the drain or collector of a transistor, and the grid is sort of like the gate or base. You will have to estimate some derivatives from the graph for this problem.
5. Look at the 2017 IEDM conference paper on the Intel 10 nm FINFET.
   a. From Figure 11, estimate g_m, r_o, and intrinsic gain for NMOS and PMOS transistors when V_{GS}=0.6V and V_{DS}=0.6V (PMOS values are negative). The current is given in mA per micron of width. You can assume a 1 um wide transistor.
   b. From Figure 11, estimate roughly what V_t is for NMOS and PMOS devices. Do these devices look quadratic, or velocity saturated? Explain your answer.
   c. From Figure 11, estimate $V_A=1/\lambda$ for NMOS and PMOS devices.
   d. From Figure 10, estimate the subthreshold slope and the parameter "n" for NMOS and PMOS devices.
   e. From Figure 8, estimate the ratio of the "on" current ($V_{GS}=V_{DS}$=0.7V) and the "off" current (V_{GS}=0V, V_{DS}=0.7V)
   f. From Figure 2, how many transistors can be made on a 1cm2 die? If all of them are "off" as defined above, what would the overall current consumption for such a chip be?
   g. If an electron is moving at the scattering limited velocity in silicon, how long does it take to cross a 10 nm channel?
6. [not graded] For a quadratic NMOS transistor with W/L=1000u/1u, with $\mu_n C_{ox}$=100μA/V^2, V_{DD}=3V, λ=1/(10V), and V_{TH}=1V.

a. Carefully sketch by hand the drain current vs. V_{DS}=0 to 3V at constant V_{GS}=0, 1, 2, 3V.
b. Do the same for a PMOS transistor of the same size with the same parameters except V_{DS}=0 to -3V and V_t=-1V. You should get exactly the same plot, just rotated 180 degrees and with different axis labels.

7. For the common source amplifier, assume $\mu C_{ox}(W/L)=2mA/V^2$, $|V_t|=1V$, and $\lambda=0.1V^{-1}$ for both devices.

A) Assuming V_{BP} = 1.9 V, calculate V_{dsatp} and I_{dp} at $V_{dp}=V_{DD}-|Vdsatp|$ for the PMOS transistor.



B) Plot |Idp| vs. Vout. What is the minimum and maximum value for Idp with the PMOS device in saturation in this circuit?

C) What is the approximate value of V_i for which the PMOS device is just on the edge between the saturation and linear regions? (you calculated the current and output voltage at which this happens in part A above). Considering just the current/ voltage relationship for the NMOS device, plot Idn at this Vi on the same plot as step B.

D) What is the value of V_i for which the NMOS device leaves saturation? Again, considering only the NMOS device, plot Idn at this value of V_i on the same plot as B.

E) Based on these values, plot V_{out} vs V_i, paying careful attention to the location of the endpoints of the high gain region (calculated in parts C and D above).

F) Based on the (Vi, Vout) pairs that you calculated in C & D, what is the gain of the amplifier? What are the input and output voltage range over which this gain is achieved.

G) Calculate the gain for this amplifier using the small signal model evaluated at the center of the high gain region. Compare to your answer in F.

8. With our simple model for the potential in the channel of a MOSFET in saturation (Week 2, Lecture 2, page 4, upper right; W2L2P4UR), assume L=1um, V_{tn}=1V, V_{GS}=1.5 V, and a silicon breakdown field E_{BD}=30V/um. At a particular drain bias ΔL=0.1um
   a. sketch the channel potential as a function of channel position x=0 to L.
   b. Calculate the drain voltage that gives this particular ΔL.
   c. What is the lateral (drain to source) electric field in the channel?
9. For an NMOS transistor with V_{tn}=1V and a 3V supply, on a plot with V_{DS} varying from 0 to 3 V on the horizontal axis and V_{GS} varying from 0 to 3 V on the vertical axis
   a. sketch the regions of operation of the quadratic model for the transistor: off, triode, and saturation.
   b. If the device has a channel length of 1 um, re-draw your plot to show the velocity saturated regions, and label the sub-threshold region
   c. Repeat part b for a PMOS device of the same length with the same magnitude of threshold voltage.