EE 140/240A Prof. Pister
Spring 2020

Homework Assignment #4

Due by online submission Thursday 2/20/2020 (Friday at 9am)

1. You have a PMOS-input common source amplifier with an NMOS load driving a capacitive load. The output is biased at mid-rail, and you can assume the quadratic model is appropriate for all parts of the problem. How do I_D, g_m, r_o, A_{v0}, w_p, w_u, input capacitance, and output swing change if you
    a. double the width of both devices
    b. double the width and length of both devices
    c. double V_{ov} in both devices
2. Problem 1, Fa09 Midterm 1. Assume that V_{tn}=-V_{tp}= 0.25 V.
3. Problem 2, Fa09 Midterm 1.
4. Using the process parameters below, design a common source amplifier with a low-frequency gain of at least 50, and a unity-gain bandwidth of 1.6 GHz while driving a 200fF load. You need an output swing of at least 1V. Make a table of W, L, ID, Vov, gm, ro, for each device, and of Av0, wp, wu, input capacitance, and output swing for the amplifier. You may assume the quadratic model for both FETs, but keep Vov greater than 100mV, and less than 1V per micron of channel length. Clearly indicate choices that you "pick" vs. things that you "calc".
    a. Is the quadratic model likely to be accurate for the bias conditions of your amplifier?
    b. If you wanted to minimize power consumption, how would your design change?
    c. If you wanted to minimize input capacitance, how would your design change?

Process Parameters: C_{ox}=5fF/um^2, C'$_{ol}$=0.2fF/um, $\mu_n C_{ox}$=200μA/V^2, $\mu_p C_{ox}$=100μA/V^2, λ= (0.1um/L)/(1V), -V_{tp}=V_{tn}=0.5V, V_{DD}=2V, L_{min}=0.1 um.

5. You make measurements on an NMOS transistor and find that with the source grounded and the drain voltage at 2V, the drain current increases from 1mA to 4mA as the gate voltage increases from 1V to 1.2V. When the gate voltage is 1.2V, the drain current increases from 4mA to 4.4mA when the drain voltage increases from 2V to 3V. Assume that the quadratic model is appropriate.
    a. What is Vtn and lambda for this device?
    b. What is K'=$u_n C_{ox}$/2 W/L?
    c. What is gm and ro when the drain voltage is 2V and the gate voltage is 1.2V? (note: use the formulas for the quadratic model and your fitting parameters)
    d. What is the intrinsic gain of the transistor at this bias point?
    e. What is the value of gm if you just calculate it from $\Delta I/\Delta V_{GS}$? Why are these two values different?
6. Given an NMOS input amplifier with an NMOS cascode and a PMOS cascode current source write a formula for
    a. G_m, the transconductance to the output
    b. G_{mc}, the transconductance to the drain of the input transistor
    c. R_o, the output impedance
    d. R_{oc}, the impedance at the drain of the input transistor
    e. the above formulas simplified assuming that $g_m r_o >> 1$ for all combinations of g_m and r_o
    f. C_{in}, the low-frequency input capacitance of the amplifier