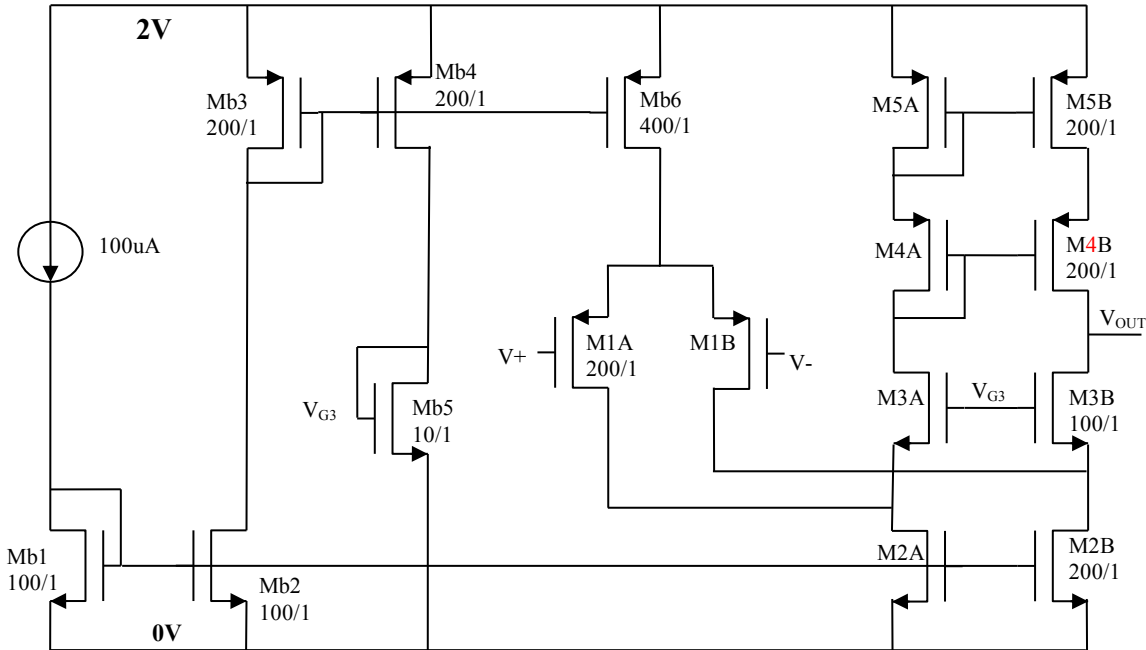


Homework Assignment #7

Due by online submission **Friday 4/3/2020** (9am Saturday)

1. 18spMid2 problem 4
2. Check out the “early op-amp” in Figure 2 on this page <https://www.maximintegrated.com/en/app-notes/index.mvp/id/4428>.
 - a. Circle and label the following components
 - i. differential pair with resistive load
 - ii. tail current sink
 - iii. common emitter gain stage with level-shifting diodes
 - iv. output stage with current-limiting resistors
 - v. Zener diode based voltage reference
 - b. Why is there a resistor in series with the Zener diode?
 - c. If the Zener has a reverse breakdown of 3.5V, and the tail resistor is 1k Ω , what is the tail current? Does it vary much with supply voltage?
 - d. If you were going to add a compensation capacitor to this op-amp, where would you put it? (draw it on the circuit)
3. Take a look at the datasheet for the TI LM324 quad op-amp. <http://www.ti.com/lit/ds/symlink/lm324.pdf> TI has been selling this op-amp for more than 40 years! (they are 10 cents each on digikey) From Figure 4 on the LM324 datasheet
 - a. estimate the slew rate in positive and negative slewing when the output load is 50pF
 - b. we haven’t studied output stages, but you can find the output current limits in the table on page 7. Is the slew rate due to the output capacitor? (hint: no. Explain why.)
 - c. What else could it be then? Estimate the size of the compensation capacitor C_c
4. The LT1008 <http://cds.linear.com/docs/en/datasheet/1008fb.pdf> (also decades old, \$3.55 on digikey) is not internally compensated. This gives you higher performance (BW, slew rate) for higher gain, but means that you need to add external capacitance when using the amplifier in low-gain configurations. They give you two choices, either add a capacitor C_F that will be somewhat Millerized or add C_s that looks more like our C_2 .
 - a. with a closed loop gain of 1,000 and perfect feedback resistor matching,
 - i. estimate your gain error at 0.1 Hz
 - ii. estimate the closed-loop pole location with $C_s=10\text{pF}$ vs. $C_F=30\text{pF}$ (page 6, lower left)
 - b. With $C_F=3\text{pF}$ vs. 30pF, what is the maximum feedback factor (and corresponding minimum gain and max bandwidth) that will give a phase margin of 60? (page 6, lower right)
5. For each of the following four op-amps, redraw the schematic of the op-amp including only those transistors that are on when the op-amp is slewing positive, and then slewing negative. (there should be 8 figures: 2 topologies, 2 types of input transistors, 2 slewing directions)
 - a. our standard 5T single-stage CMOS op-amp, with NMOS input, and with PMOS input
 - b. the current mirror op-amp, with NMOS, and with PMOS
6. For a two-stage NMOS-input CMOS op-amp with the output stage biased at 100 μA and the tail current at 10 μA
 - a. calculate the positive and negative slew rate if $C_c=1\text{pF}$ and $C_L=1\text{pF}$.
 - b. calculate the positive and negative slew rate if $C_c=1\text{pF}$ and $C_L=100\text{pF}$.
7. For a two-stage NMOS-input CMOS op-amp with the output stage biased at 100 μA and the tail current at 10 μA with $C_c=1\text{pF}$ and $C_L=100\text{pF}$., assume a 5V supply, 1 V threshold voltages, and 100mV overdrive voltages for all transistors. With the op-amp in unity gain feedback,
 - a. on a single plot carefully sketch the output voltage of the first and second stage vs. time when the input makes a step change from 2 V to 4 V. Your plot should clearly show initial and final values, and rates of change. Calculate the rate of change of the voltage on C_c . You only need to show the slewing behavior, but estimate the voltage and time at which the op-amp stops slewing.

- b. repeat, for an input transition from 4 V to 2 V.
8. If the previous op-amp had an open-loop phase margin of 70 degrees, a gain of 10,000, and a pole at 1,000 rad/s
- What is the open-loop unity gain frequency?
 - What is the closed-loop pole frequency and time constant
 - If the desired settling error is 0.1 mV, how many time constants are needed to settle?
 - Compare the slewing time to the settling time
9. Given the choice of NMOS or PMOS input stage, and the five different op-amp topologies that we've talked about (single-stage 5T diff pair with mirror load, single-stage current mirror, two-stage, telescopic cascode, folded cascode), which combinations are appropriate for the following applications? Assume that the magnitude of the N and P threshold voltages is roughly $\pm 0.6V$, and that all overdrive voltages are at least 0.1V.
- bandgap reference as in Figure 4.46c driving a 100 k Ω load
 - digital voltage regulator with an output of 1V and a supply of between 1.6 and 3.2V
 - analog voltage regulator with an output of 1.25V and a supply of between 1.6 and 3.2V
 - ADC comparator with an input at 1.25V and a supply at 1.25V
 - variable gain amplifier with an input at 0V and a supply at 1.25V
10. For the PMOS-input folded cascode op-amp below, assume the quadratic model with the following process specs $\mu_n C_{ox} = 200 \mu A/V^2$, $\mu_p C_{ox} = 100 \mu A/V^2$, $\lambda = 1/(10V)$, $-V_{tp} = V_{tn} = 0.3V$, $C_{ox} = 5fF/\mu m^2$, $C'_{ol} = 0.5fF/\mu m$.



- Calculate and tabulate:
 - the overdrive voltage and current in all devices. For this step you may assume that $\lambda = 0$. The simplest order may be Mb1 through Mb6, then M1 through M5.
 - Calculate the bias voltages on all nodes, assuming $V_{I,CM} = 1V$. Specifically: tail, G2, G3, G5, G6, S3B, S4AB, and out.
 - the g_m and r_o parameters for M1 through M5
 - Calculate G_m , R_o , and A_v
 - Calculate the input common mode range and output swing.
 - What is the minimum voltage that could be used on the gates of M3AB to still keep M2AB in saturation? If you used that voltage, what is the new input common mode range and output swing? How would you change the size of Mb5 to achieve that voltage?
 - If the load capacitance is 1pF (roughly the same as the input capacitance),
 - what are the pole and unity gain frequencies?
 - What is the phase margin in unity gain?
 - What are the frequencies of the pole/zero doublets from the current mirror?
11. To increase the positive output swing of the previous amplifier,

- a. redraw the PMOS current mirror M4AB, M5AB as a high-swing cascode current mirror, as in Figure 5.18b in Razavi (5.13b in the 1st edition), but PMOS.
- b. Generate V_b (V_{G4}) using something like Mb5 above, but PMOS. What current source do you use? What gate voltage biases it? What W/L do you use for all devices, and why?
- c. [240A] generate V_b from the circuit suggested in 5.19b in Razavi. What value for $(W/L)_5$ in that figure is needed?

12.