EE 140/240A Linear Integrated Circuits
Spring 2020   Lab 4

1 Introduction

For this lab, you may consult the professor, the TAs, your friends, the textbook, the internet, and any other living or inanimate objects, with the exception of your peers' lab reports. You must **submit your own written report**. Be concise. Hand calculations should be to 1 or at most 2 digits of precision.

2 Objective: Process Characterization and PVT-Insensitive Biasing

For each problem you will be exploring the models of several different devices: short channel and long channel, NMOS and PMOS, and different flavors of devices (low-threshold, regular threshold voltage, and higher voltage tolerance).

	$\frac{W}{L}$
short channel	$10L_{\min}/L_{\min}$
long channel	$10\mu m/1\mu m$

In general you will have eight answers to each question, e.g. "Low-V_t PMOS short channel look quadratic over the range…, Regular-V_t NMOS long channels look quadratic over the range…," etc. You may find it easiest to plot each device on a different plot.

3 Prelab: Process Characterization

For the prelab, you can work in groups of 4 and each characterize 2/8 devices to get all the data.

(1) With $|V_{ds}| = 1.5$V, use Cadence to simulate I_d vs. V_{gs} for V_{gs} from 0V to $V_{DD} = 1.8$V. Do this for devices `ne`, `nel`, `pe`, and `pel`. The "ℓ" stands for "low threshold voltage", or LVT. **Note that the minimum channel lengths of low-Vt and regular-Vt devices are different**

    a. Plot all of the currents. Do the short channel devices look like our velocity saturation model? Do the long channel devices look quadratic? Over what range of V_{gs} for each?

    b. Over the range where the device looks velocity saturated (if any), estimate $C_{ox}v_{scl}$ and V_t.

    c. Plot $\sqrt{I_d}$. What is the range of V_{gs} for which the curves look linear? For that range, estimate μC_{ox} and V_t. Hint: Remember that you can use Cadence's built-in calculator!

    d. Compare your estimates of V_t for each device from parts 1.b and 1.c.

    e. Plot $\log_{10}(I_d)$. What is the range over which each curve looks straight? Estimate the non-ideality factor n and $\frac{I_s}{W}$ for each subthreshold model in those regions.

    f. Plot g_m for all devices vs. V_{gs}. Which device, at what bias point, gives the best g_m? *Hint:* $g_m = \frac{\partial I_d}{\partial V_{gs}}$. *Remember the* `deriv` *function from Lab 2?*

g. Plot $\frac{g_m}{I_d}$ for all devices vs. V_{gs}. How does this compare to theory for sub-threshold, quadratic, and saturation models? Where are the transitions?

h. Which device, at what bias point, gives the best g_m per µA? This is one of the most important metrics of performance.

(2) For the same devices as above, simulate I_{ds} vs. V_{ds} from V_{ds} from 0V to $V_{DD} = 1.8$V with $|V_{gs}| = 1.0$V.

a. Plot I_{ds} and r_o on the same plot.

b. Is there a clear transition to saturation for each device? Does it happen where you expect, relative to the V_t values calculated above?

c. Try to pick the best value for λ that you can, and sketch by hand what you expect. Is $r_o = \frac{1+\lambda V_{ds}}{\lambda I_d}$ a good model for output resistance for any/some/all of these devices?

d. Which device, at what bias point, gives the highest intrinsic gain?

(3) Now for the devices `ne5` and `pe5`, tabulate the following

- Over what V_{GS} region the devices look quadratic or velocity saturated in the same fashion as 1.a
- $C_{ox} v_{scl}$ for devices when they're velocity saturated
- V_t
- μC_{ox}
- The nonideality factor n and I_S/W
- A plot of g_m/I_D
- λ

with the new parameters:

Parameter	Value
V_{DD}	5V
V_{DS}	4.5V
$\left(\frac{W}{L}\right)_{short}$	$\frac{5\mu m}{500nm}$
$\left(\frac{W}{L}\right)_{long}$	$\frac{50\mu m}{5\mu m}$

(a) I_D vs. V_{GS} parameters

| Parameter	Value
V_{DD}	5V
V_{GS}	1.5V
$\left(\frac{W}{L}\right)_{short}$	$\frac{5\mu m}{500nm}$
$\left(\frac{W}{L}\right)_{long}$	$\frac{50\mu m}{5\mu m}$

(b) I_D vs. V_{DS} parameters

(4) Estimate C_{gs} for each device. *Hint: Small signal $\frac{i_d}{i_g} = 1$ when $\omega = \frac{g_m}{C_{gs}}$!*

Estimate the unity gain frequency for each device in a common source amplifier with an ideal current source load when driving a copy of itself.

4 Lab: Current References

4.1 Current References

The simple resistor-biased current mirror is included as a control to see how bad things can be. The constant-g_m is a step in the right direction, and is good enough for some applications.

(a) Resistively biased current mirror

(b) The "constant g_m" reference circuit
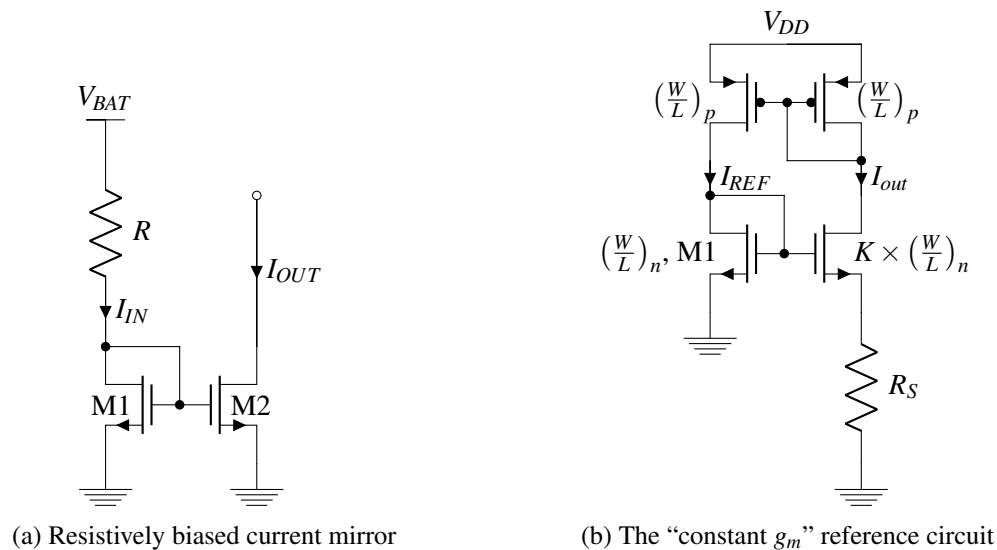
- Design both circuits to have a nominal output current $I_{OUT} = 10\mu A$.

- Plot the output current and gate bias voltage on M1 in both circuits vs. temperature and battery voltage. You can set up a DC sweep for temperature and use Parametric Analysis or ADE XL to vary battery voltage from 0.8V to 1.6V in steps of 200mV.

- Tabulate the worst-case variation.
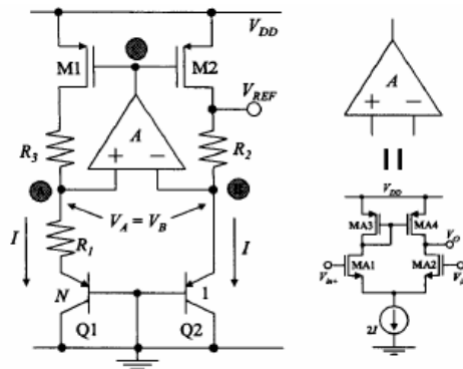
4.2 Bandgap Reference

Figure 2: Mok, Philip KT, and Leung, Ka Nang. "Design Considerations of Recent Advanced Low-Voltage Low-Temperature-Coefficient CMOS Bandgap Voltage Reference." Custom Integrated Circuits Conference, 2004. http://web.mit.edu/Magic/Public/papers/IEEEXplore(14).pdf

Now you will design the bandgap circuit shown above to generate $V_{REF} = 1.2V$.

- We'll set $R_3 = R_2$.

- **We highly recommend putting your op amp in a separate cell so you can test it in isolation before putting it in your bandgap circuit.** Your op amp may be a simple differential pair or a two-stage op amp. It needs to run off of V_{BAT} because at this point you don't have any other voltages to work from.

- The bipolar PNP transistors are actually diodes. Use any diode or bipolar element you please from the xt018 toolkit. Make Q1 and Q2 the same dimensions and then use the "multiplier" field to put copies of each in parallel. The ratio of the size of Q1 to Q2 should be a rational number.

- The resistors should have a temperature coefficient. You can start with analogLib resistors, but you must replace them with your choice of resistor (except pfuse) from the xt018 toolkit.

- Show that the current in both branches is

$$I = \frac{\Delta V_{BE}}{R_1}$$

- Write an expression for V_{REF} in terms of ΔV_{BE}, V_{BE}, R_1, and R_2.

- Now rewrite your expression for V_{REF} in terms of I_s, V_{BE}, V_t, R_1, R_2, and N.

- Now choose values for N and for the ratio of $\frac{R_2}{R_2}$ to get close to a zero temperature coefficient. Use only rational numbers for N and the ratio. We do this so that we make the resistors and capacitors match very well during layout by constructing them from unit elements.

- Choose a starting size for Q2. We will iterate and adjust this later.

- Calculate what V_{BE2} should be in order to generate $V_{REF} = 1.2$V given your previous choices.

- Simulate a copy of the Q2 diode to find how much current is required to give the value of V_{BE2} you calculated.

- Calculate the size of R_2 now that you know the current through it and voltages across it.

- Calculate the size of R_1 using the ratio you picked earlier. Note that we have a tradeoff here between the size of the resistors and the bias current through the diodes. If your resistors are extremely large (many MΩ), you can adjust your diode size and recalculate.

- Size the PMOS transistors to deliver the calculated current with an overdrive of a few hundred millivolts.

- Now that you have finished sizing all the components, you can return to your choices made earlier and adjust if necessary.

- Set a value for V_{BAT} and run a DC simulation sweeping the temperature from $-40°$C to $+85°$C. Plot V_{REF}.

- Ideally the output should look parabolic with a slope of zero near 25°C. You will likely need to make adjustments.

- If you need to make adjustments, think about what the slope of your output is telling you. You likely have too much of either the positive temperature coefficient or the negative. Make adjustments to balance these so they add up to zero near 25°C.

- Once you have a relatively flat temperature response, rerun the simulation varying V_{BAT} from 0.8V to 1.6V in steps of 200mV.

4.3   Bandgap Startup and Stability

So far we've only checked our bandgap in DC simulations. It's important to make sure that when power is first applied the circuit begins to properly operate and that it is stable.

- Using "vpulse" from analogLib for V_{BAT} to create a linear voltage ramp from 0V to 2.4V with a rise time of 100ns

- Run a transient simulation

- Your circuit should properly start up and settle to V_{REF}. If it doesn't (e.g. it starts oscillating), add compensation capacitance to stabilize it.

- How long does your circuit take to start up and settle within 10% of the final value?

5   Deliverables

Your final schematics should have no analogLib components.

Do not use default Cadence plots for submission. You should either

- Export and plot with Python, MATLAB, Excel, etc. with readable axis labels

- Modify your Cadence plot settings:
  - Graph $\rightarrow$ Properties $\rightarrow$ Set background to white
  - Graph $\rightarrow$ Properties $\rightarrow$ Graph Options $\rightarrow$ Font $\rightarrow$ Fixed [Sony] $\rightarrow$ Size 18
  - Right click on traces $\rightarrow$ Width $\rightarrow$ Extra Thick

Do not use Cadence schematics for submission. You should either

- Draw neatly by hand

- Use some nice schematic drawing software (circuitikz in LaTeX, Adobe Illustrator, Digi-Key Scheme-It, etc.)

(1) Current Mirror & Constant g_m

     a. Schematic of simple current mirror with sizes annotated

     b. Schematic of constant g_m with sizes annotated

     c. Plot of output current and V_{G1} vs. temperature and V_{BAT} for the simple current mirror

     d. Plot of output current and V_{G1} vs. temperature and V_{BAT} for the constant g_m

     e. Tabulate variation of I_{OUT} from the ideal at the corners (min/nominal/max temperature, min/nominal/max battery voltage)

     f. Worst-case variation of I_{OUT} from the ideal with information on what temperature and battery voltage it occurred at

(2) Bandgap Reference

    a. Schematic of bandgap reference with sizes annotated (including op amp schematic)

    b. Plot of V_{REF} vs. temperature and battery voltage

    c. Tabulate variation of V_{REF} from the ideal 1.2V across temperature and battery voltage

(3) Bandgap Startup and Stability

    a. Transient bandgap showing stable startup, annotated with the time when it settles within 10% of final value